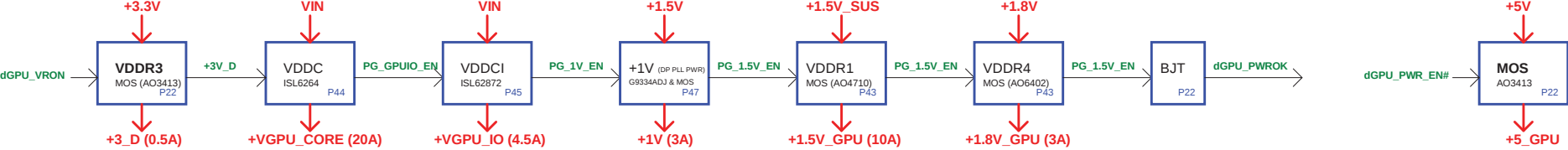
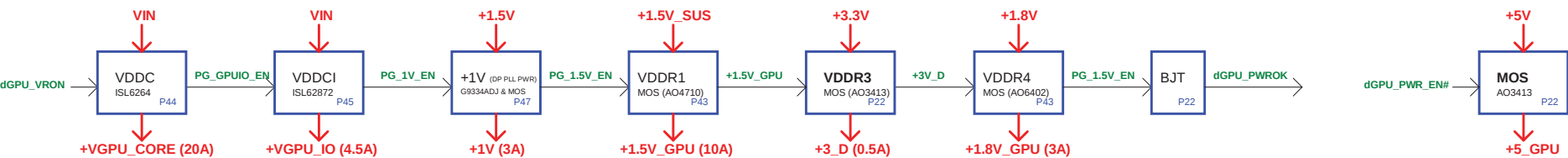


GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDR3)



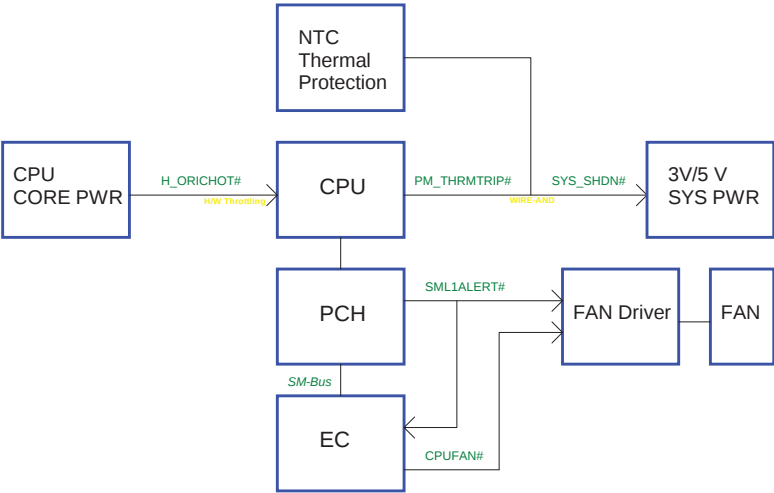
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)

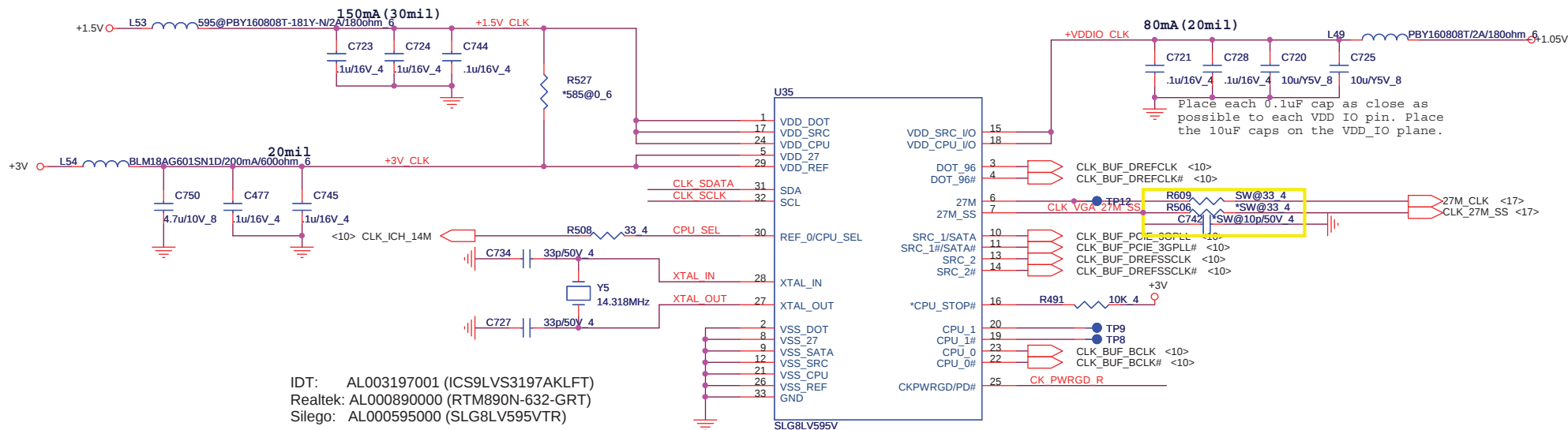


Power States

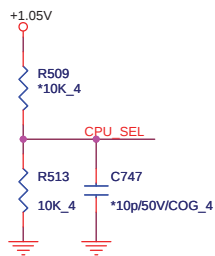
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



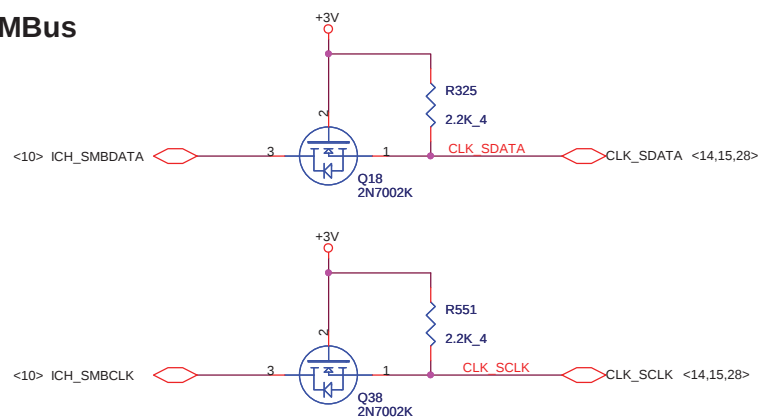


CPU_CLK select

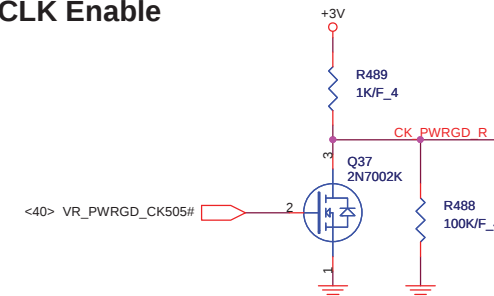


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus

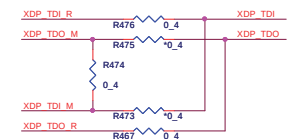
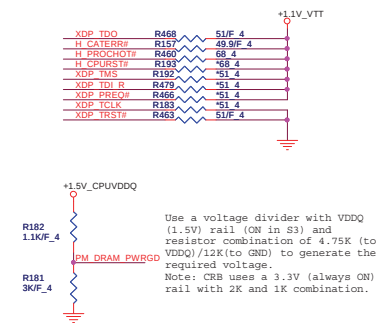
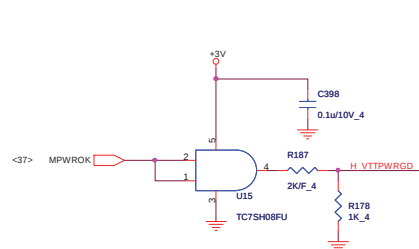
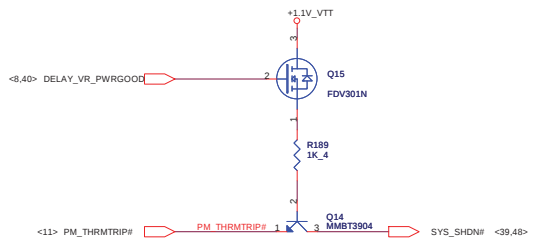
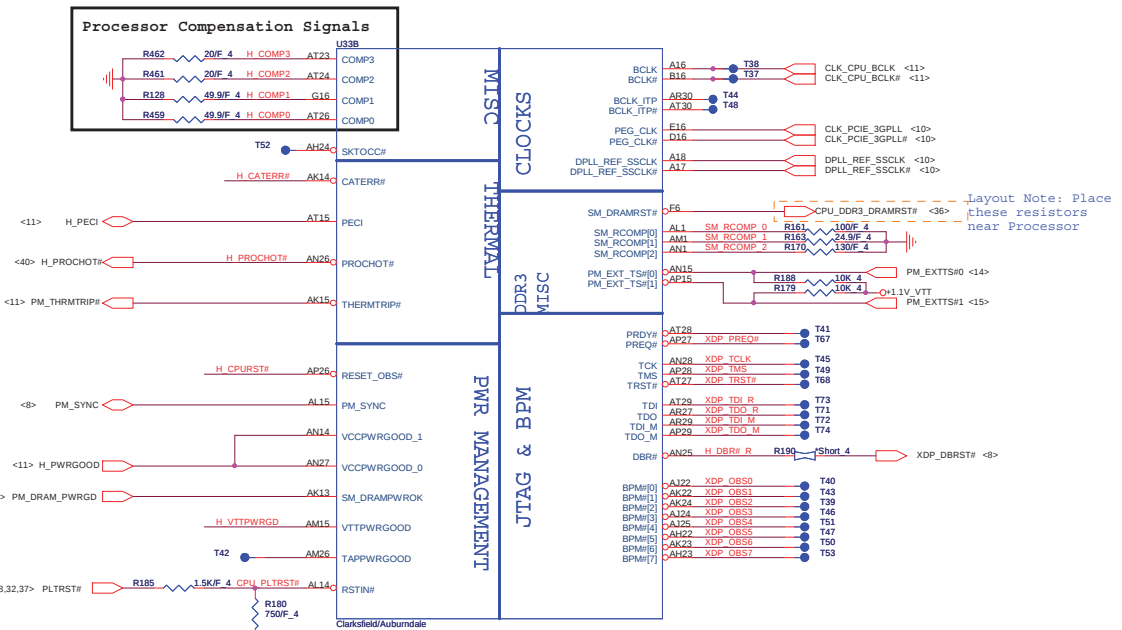


CLK Enable



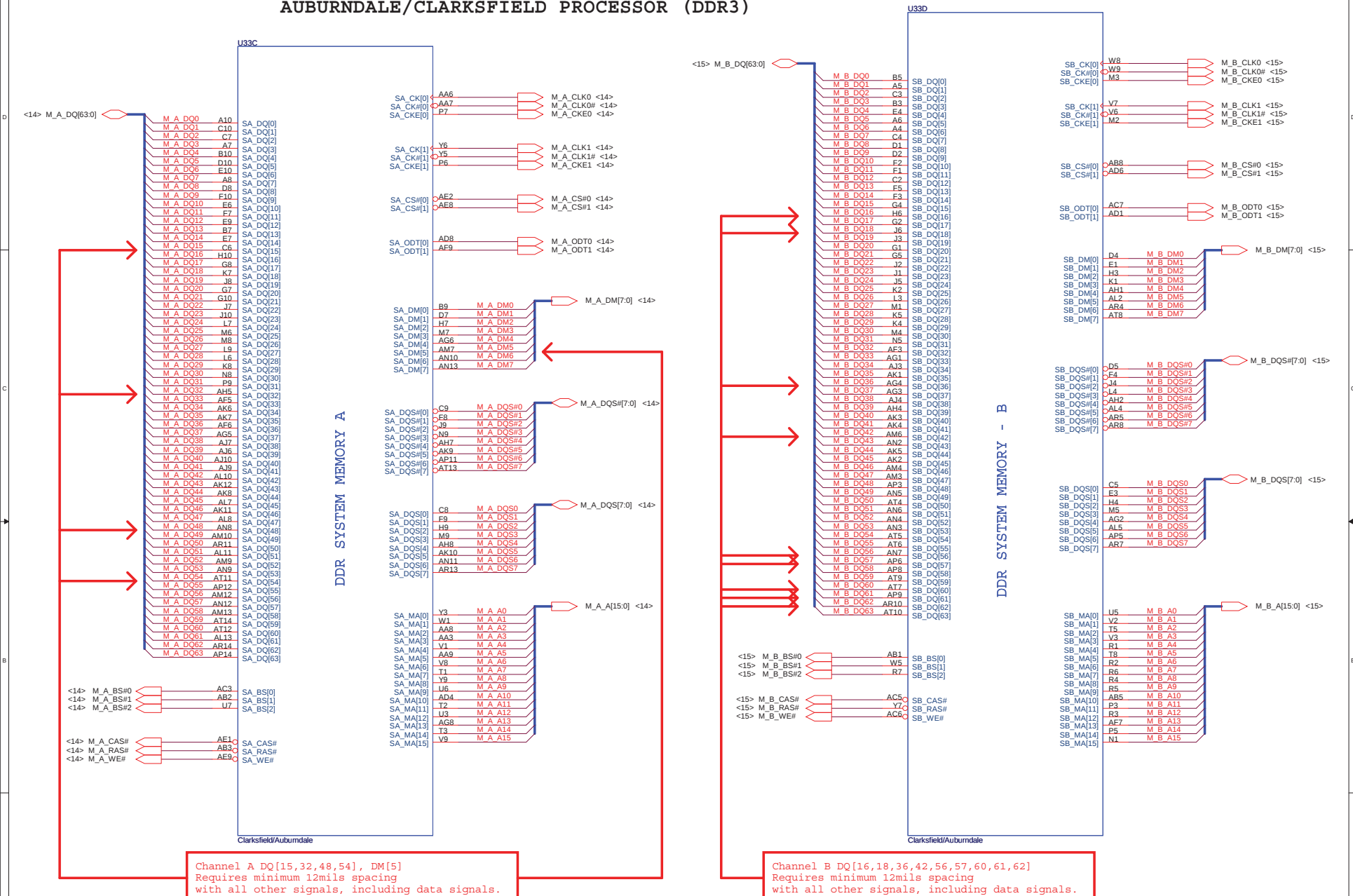
Quanta Computer Inc.
PROJECT : ZR7B

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	Clock Generator	1A
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Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

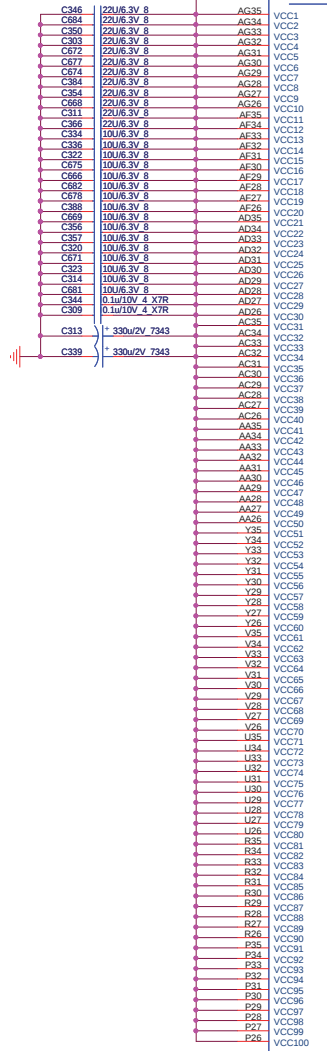


CPU Core Power

US3F

ARD:48A
CFD:52A

+VCC CORE



CPU CORE SUPPLY

POWER

CPU VIDS

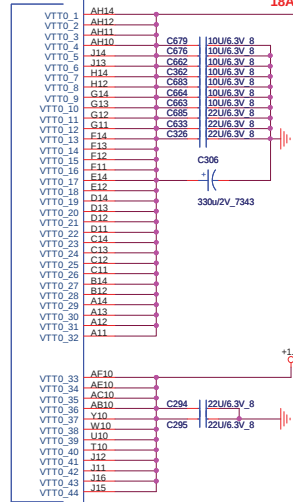
SENSE LINES

Clarkfield/Auburndale

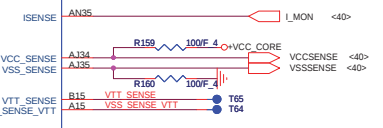
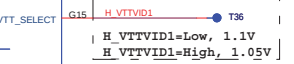
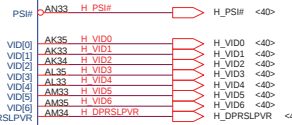
VTT Rail Values are
Auburndale VTT=1.05V
Clarkfield VTT=1.1V

18A

+1.1V_VTT

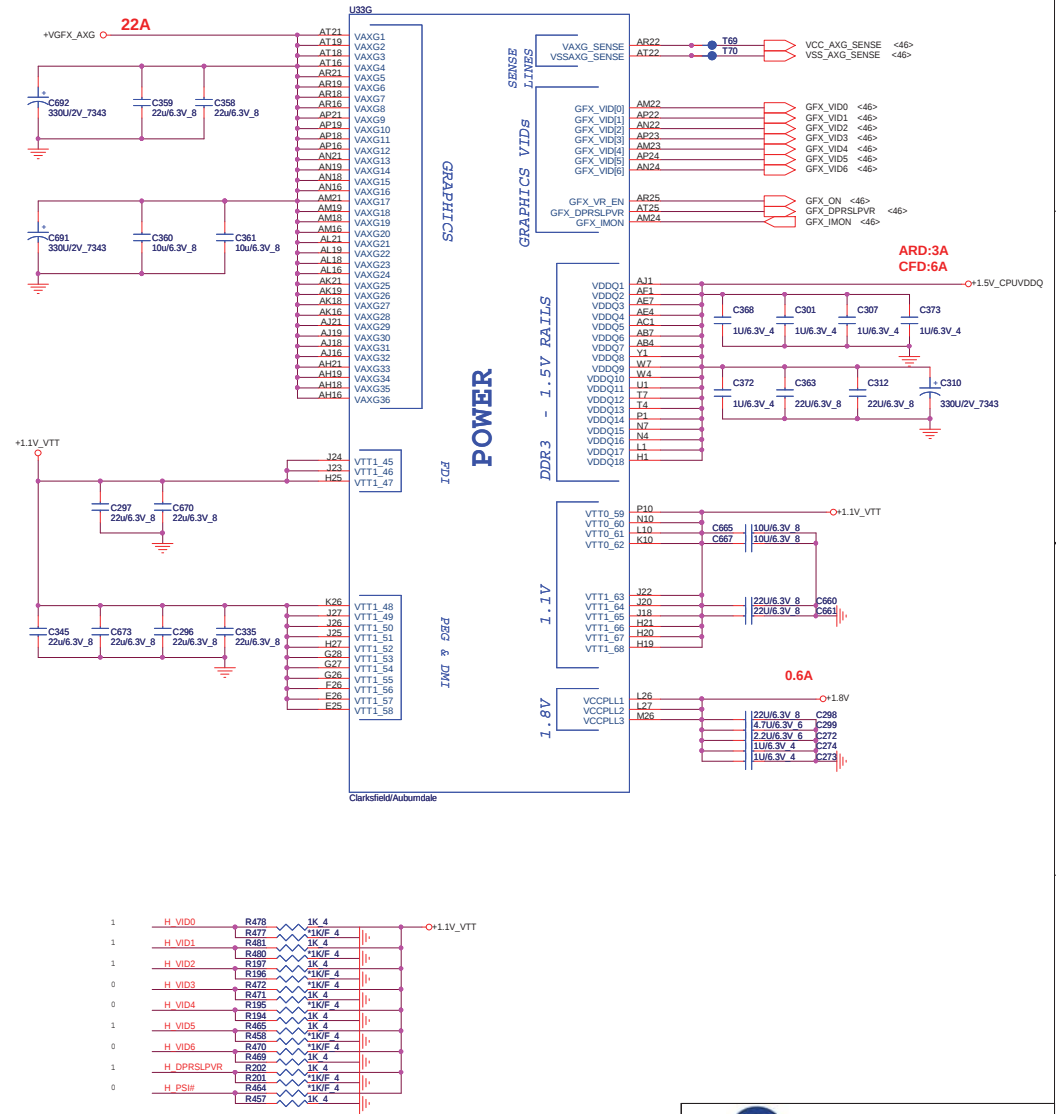


+1.1V_VTT



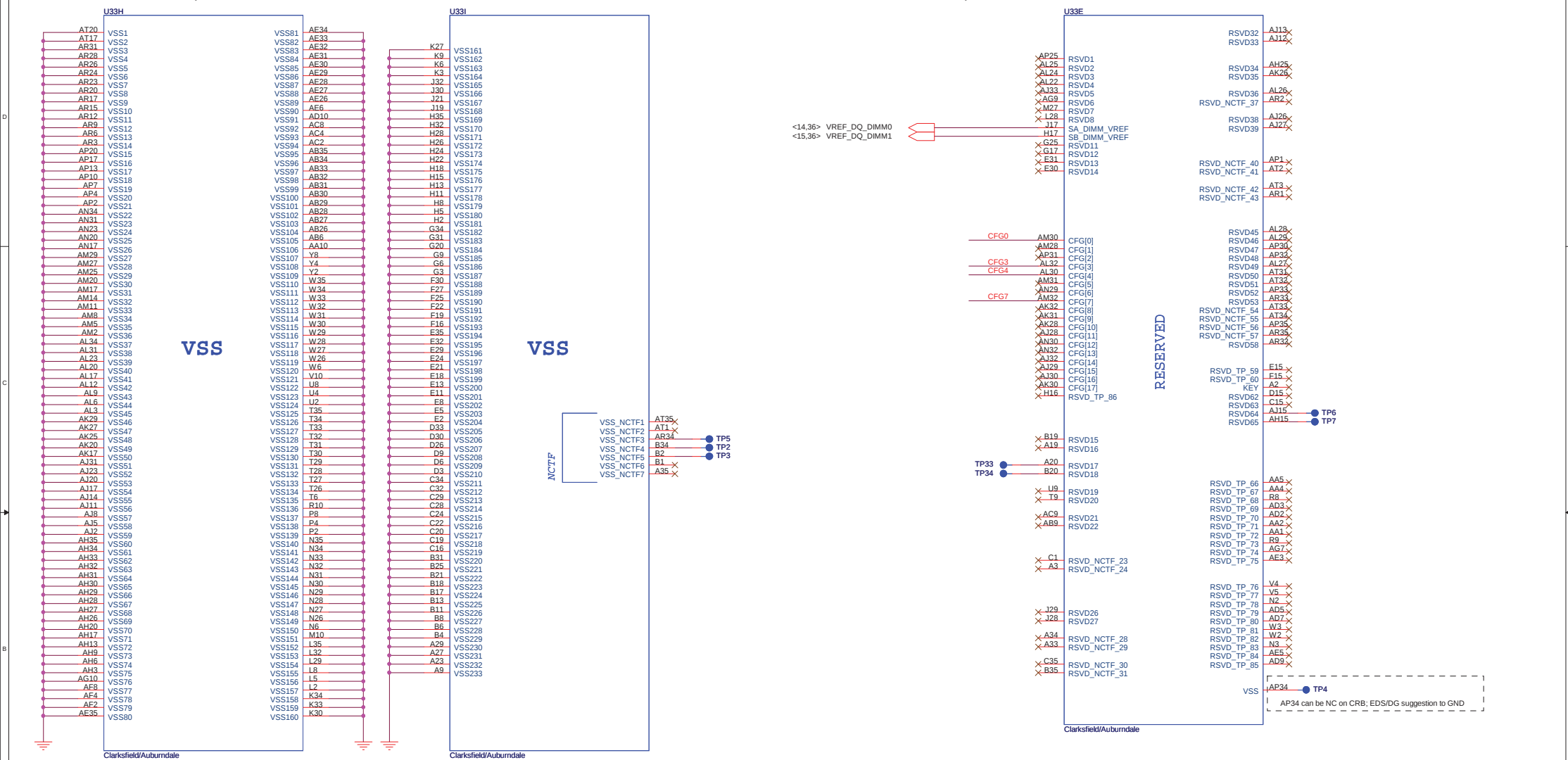
AUBURNDAL/CLARKSFIELD PROCESSOR (POWER)

AUBURNDAL/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

H_VID0 : Max 1.4V
LFM_VID : Min 0.65V

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

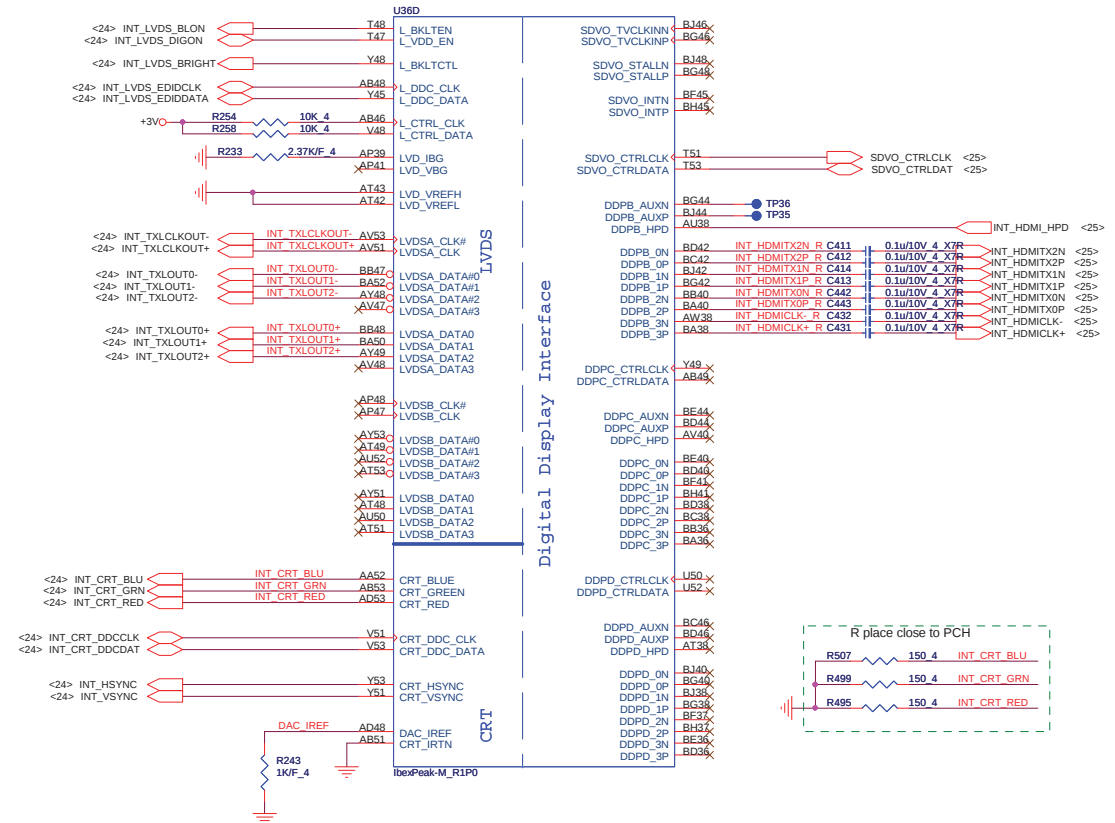
AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)



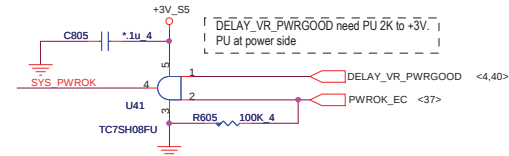
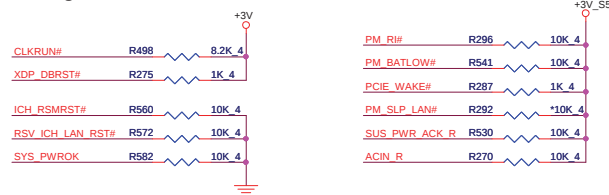
Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R186 $\sim$ 3.01K NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R169 $\sim$ 3.01K/F 4
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R162 $\sim$ 3.01K
T h b e t p e t p e				CFG7 R172 $\sim$ 3.01K/F 4

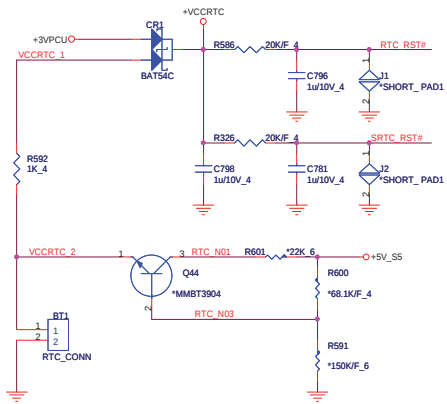
IBEX PEAK-M (LVDS, DDI)



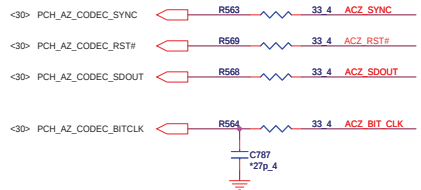
System PWR_OK



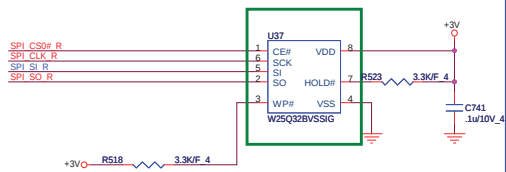
RTC Circuitry



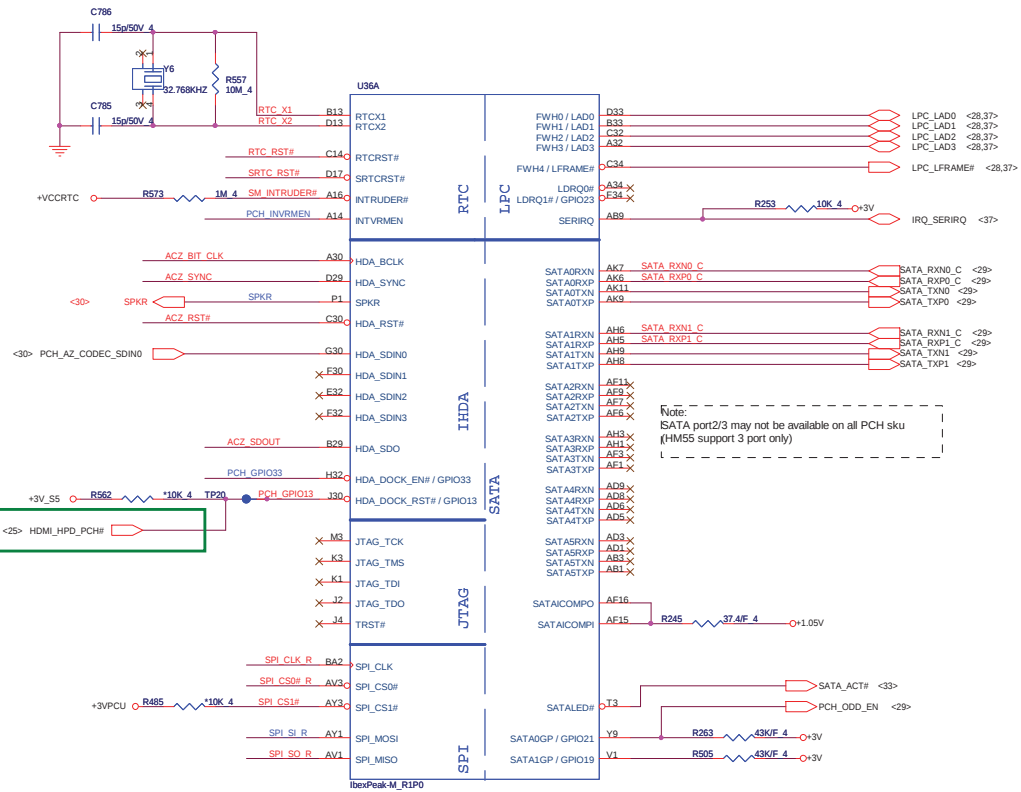
HDA Bus



PCH SPI

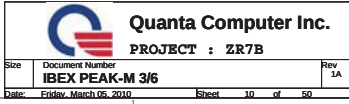


HDA_SYNC (PCH strap pin)
Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V



PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R593 330K 6 PCH INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R529 1K 4 SPI SI R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R522 1K/F 4 SPKR
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R296 1K/F 4 R296 1K/F 4
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	R455 1K 4 R455 1K 4 R455 1K 4
GNT2#/ GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	<10,26> PWM_SELECT# R289 1K/F 4
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	<3> PCI_GNT3# R528 10K/F 4
NV_ALE	Intel® Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	<10> NV_ALE R225 1K/F 4 +1.8V
NV_CLE	DMI Termination voltage. Weak internal pull-up. Do not pull low.	DMI termination voltage. Weak internal pull-up. Do not pull low.	<10> NV_CLE R224 1K/F 4 +1.8V
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low!	+3V_GPIO8 R302 10K 4 +3V_SS R296 1K 4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	CR_WAKE# R266 1K 4 +3V_SS
GPIO27	On-Die PLL Voltage Regulator <Internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	<11> PCH_GPIO27 R247 10K 4



The diagram illustrates the internal wiring and component layout of the iBexPeak-M R1P0 board. It is divided into several functional sections:

- U36F:** Contains various control and status signals such as `BMBUSY#`, `SIO_EXT_SMI#`, `SIO_EXT_SCI#`, `BOARD_ID0`, `RSV_GPIO8`, `LAN_DISABLE#`, `CR_WAKE#`, `dGPU_PWROK`, `GPIO22`, `PCH_GPIO27`, `TP_PCH_GPIO28`, `STP_PC#`, `dGPU_VRON`, `dGPU_PWR_EN#`, `dGPU_PRSENT#`, `SAVE_LED#`, `RST_GATE#`, `SV_SET_UP`, `SATA5GP`, and `GPIO57`.
- MISC:** Includes signals like `CLKOUT_PCIE6N`, `CLKOUT_PCIE6P`, `TACH1 / GPIO1`, `TACH2 / GPIO6`, `TACH3 / GPIO7`, `GPIO8`, `LAN_PHY_PWR_CTRL / GPIO12`, `GPIO15`, `SATA4GP / GPIO16`, `TACH0 / GPIO17`, `SCLOCK / GPIO22`, `GPIO24`, `GPIO27`, `GPIO28`, `STP_PC# / GPIO34`, `SATACLKREQ# / GPIO35`, `SATA2GP / GPIO36`, `SATA3GP / GPIO37`, `SLOAD / GPIO38`, `SDATAOUT0 / GPIO39`, `PCIECLKRQ6# / GPIO45`, `PCIECLKRQ7# / GPIO46`, `SDATAOUT1 / GPIO48`, `SATA5GP / GPIO49`, and `GPIO57`.
- GPIO:** A central section for general-purpose input/output pins, including `GPIO1` through `GPIO57`.
- CPU:** Contains signals related to the CPU, such as `CLKOUT_BCLK0_N / CLKOUT_PCIE8N`, `CLKOUT_BCLK0_P / CLKOUT_PCIE8P`, `PECI`, `RCIN#`, `PROCPWRGD`, `THRMTRIP#`, `TP1`, `TP2`, `TP3`, `TP4`, `TP5`, `TP6`, `TP7`, `TP8`, `TP9`, `TP10`, `TP11`, `TP12`, `TP13`, `TP14`, `TP15`, `TP16`, `TP17`, `TP18`, `TP19`, `TP20`, `TP21`, `TP22`, `TP23`, `TP24`, `TP25`, `TP26`, `TP27`, `TP28`, `TP29`, `TP30`, `TP31`, `TP32`, `TP33`, `TP34`, `TP35`, `TP36`, `TP37`, `TP38`, `TP39`, `TP40`, `TP41`, `TP42`, `TP43`, `TP44`, `TP45`, `TP46`, `TP47`, `TP48`, `TP49`, `TP50`, `TP51`, `TP52`, `TP53`, `TP54`, `TP55`, `TP56`, `TP57`, `TP58`, `TP59`, `TP60`, `TP61`, `TP62`, `TP63`, `TP64`, `TP65`, `TP66`, `TP67`, `TP68`, `TP69`, `TP70`, `TP71`, `TP72`, `TP73`, `TP74`, `TP75`, `TP76`, `TP77`, `TP78`, `TP79`, `TP80`, `TP81`, `TP82`, `TP83`, `TP84`, `TP85`, `TP86`, `TP87`, `TP88`, `TP89`, `TP90`, `TP91`, `TP92`, `TP93`, `TP94`, `TP95`, `TP96`, `TP97`, `TP98`, `TP99`, `TP100`.
- NCTF:** Contains signals like `VSS_NCTF_1` through `VSS_NCTF_31`.
- RSVD:** Reserved signals, including `INIT3_3V#`.

The diagram also shows various components like resistors, capacitors, inductors, and integrated circuits. It includes a note about the `TEMP_ALERT#` signal being used for CPU or Graph/Memory temperature monitoring and a warning to avoid this signal for other purposes.

Pin	Signal	Resistance	Value
TP_PCH_GPIO28	R511	10K	4
GPIO45	R537	10K	4
RST_GATE#	R322	10K	4
GPIO57	R309	10K	4
LAN_DISABLE#	R279	10K	4
+3V S5			
+3V			
SIO_EXT_SMI#	R299	10K	4
SIO_EXT_SCI#	R570	10K	4
dGPU_PWR_EN#	R251	10K	4
+3V			
SIO_RCIN#	R515	10K	4
SIO_A20GATE	R514	10K	4
dGPU_HOLD_RST#	R246	10K	4
SATA5GP	R250	10K	4
GPIO22	R262	10K	4
SAVE_LED#	R521	10K	4
STP_PCI#	R274	10K	4
GPIO38	R497	10K	4
BMBUSY#	R252	8.2K	4
SV_SET_UP	R257	10K	4

GPIO57 stuff PD and not stuff PU for Intel_suggestion at 6/1

GPIO57

R301 10K 4

R575 10K 4 BOARD ID0

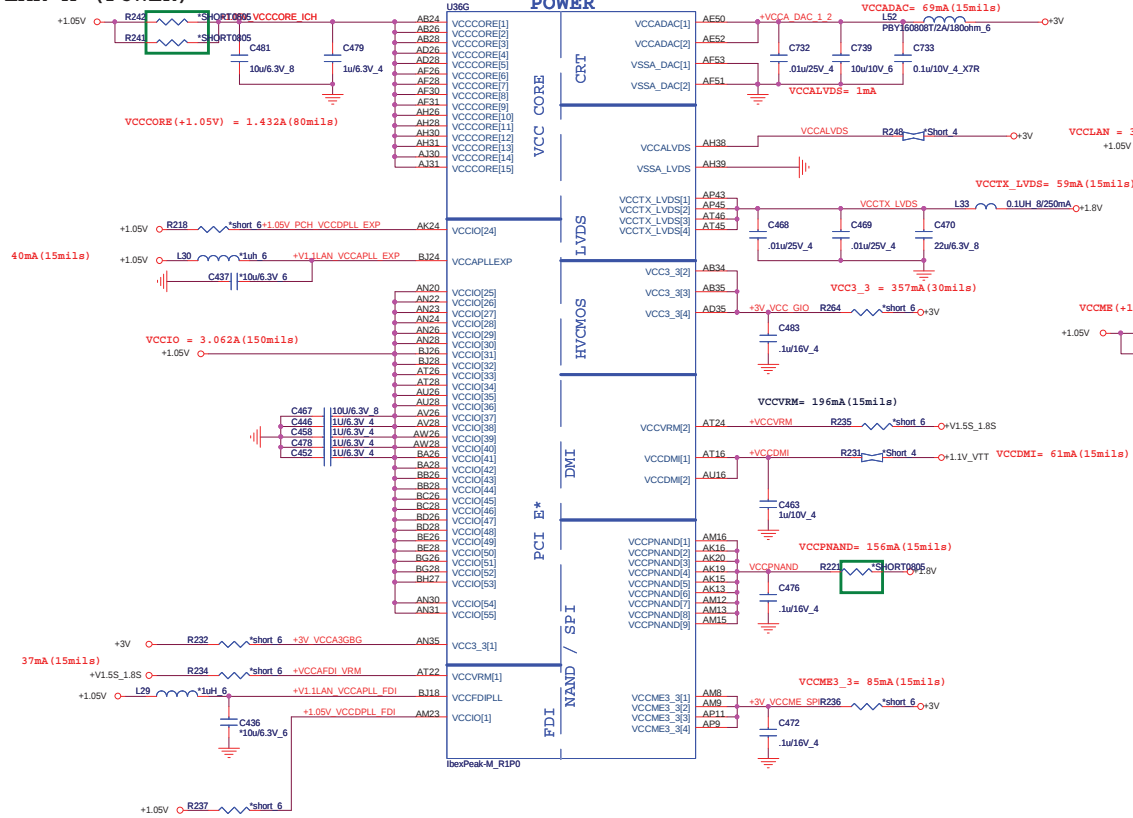
R579 10K 4

R239 10K 4 SW@10K 4

dGPU always exist

BOARD_ID0	High = JV41/JM41 Low = JM51
RSV_GPIO8	High = Disable Low = Enable

IBEX PEAK-M (POWER)

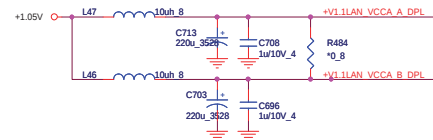


```
| VRM enable by strap pin GPIO27
| which supply clean 1.05V for
| [VCCACLK,VCCAPLLEXP,VCCFDIPLL,VCCSATAPLL]
```

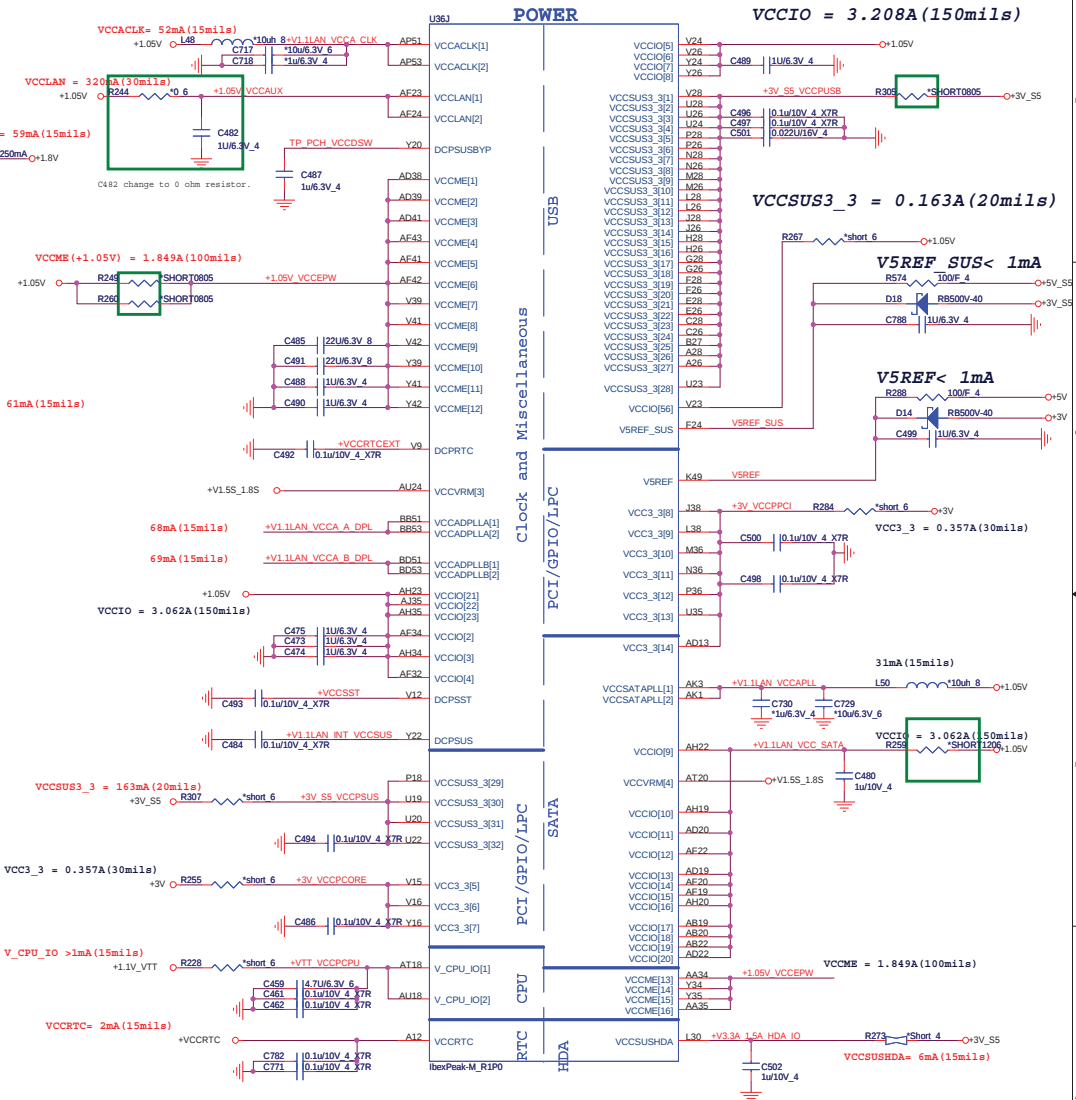
VCCVRM=196mA(15mils)

HDA_SYNC (PCH strap pin)

```
Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V
```



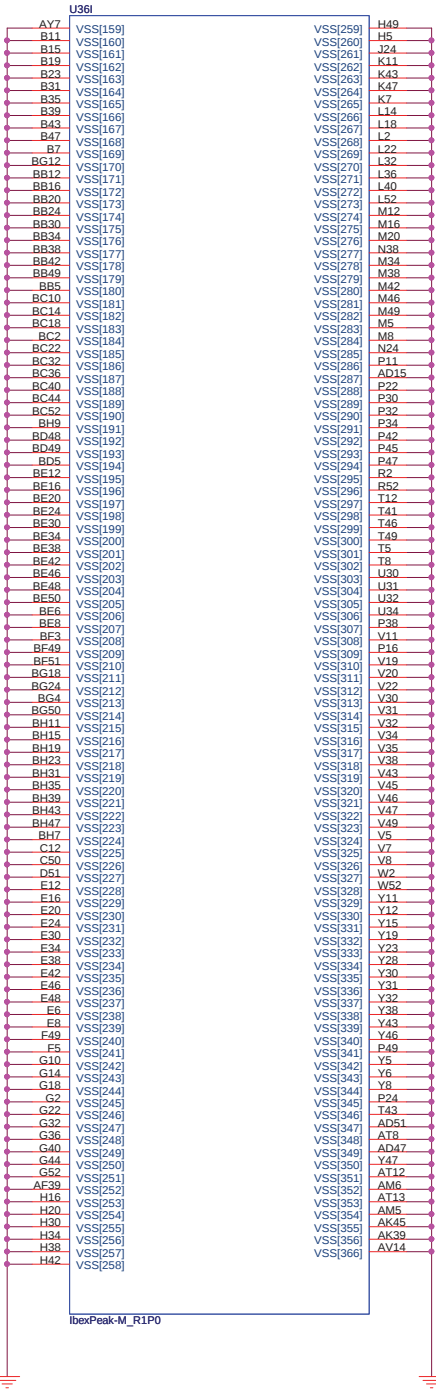
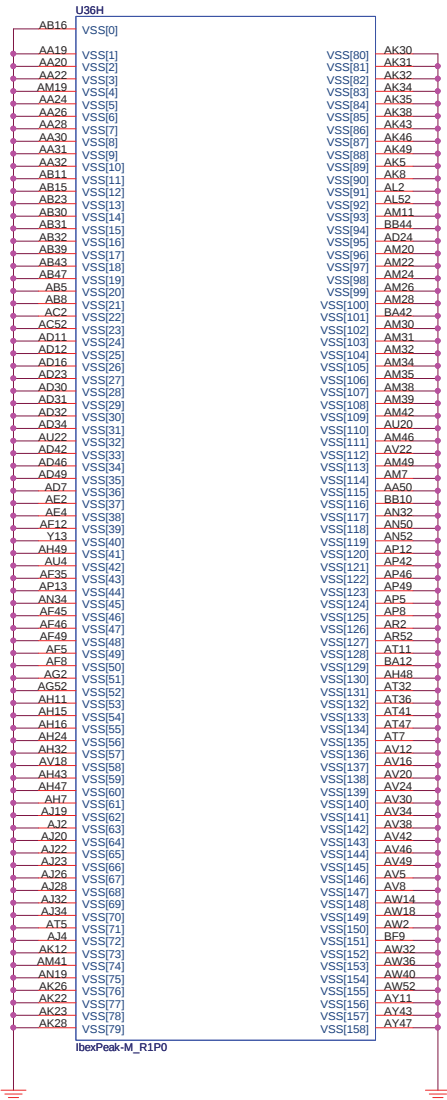
POWER



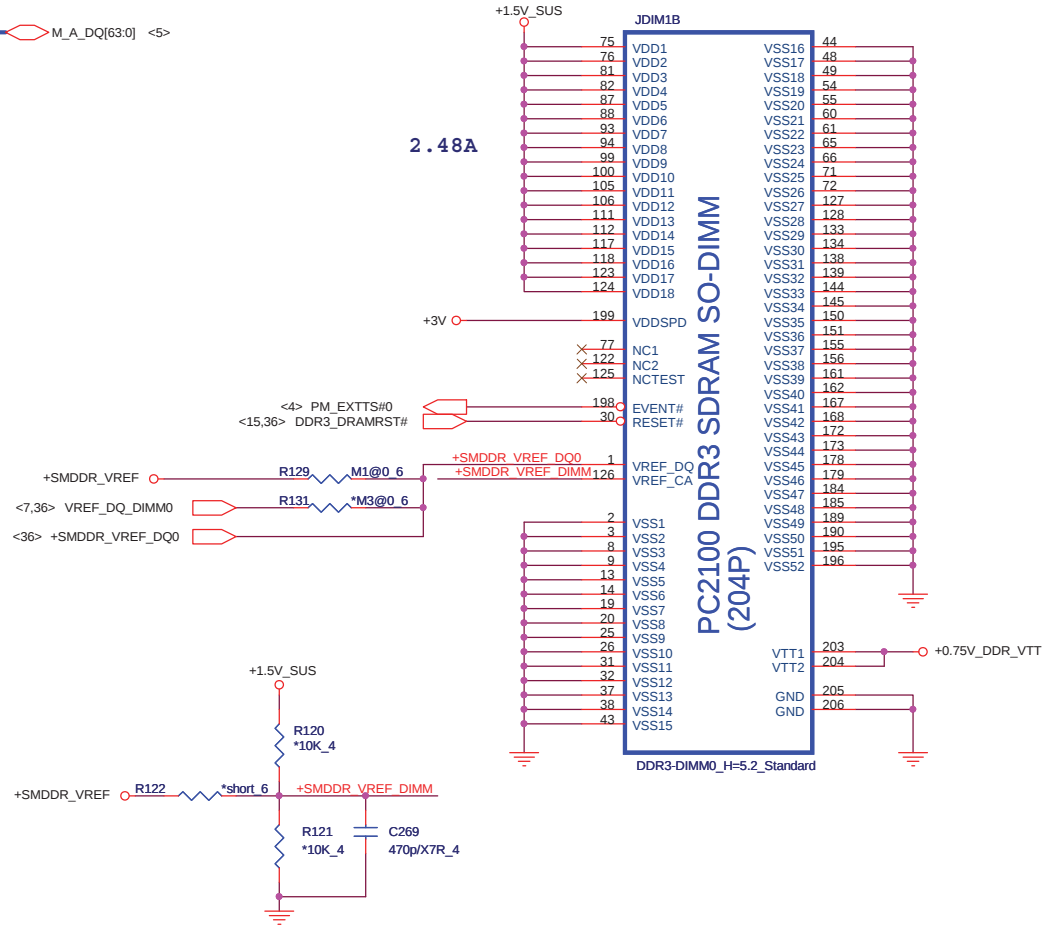
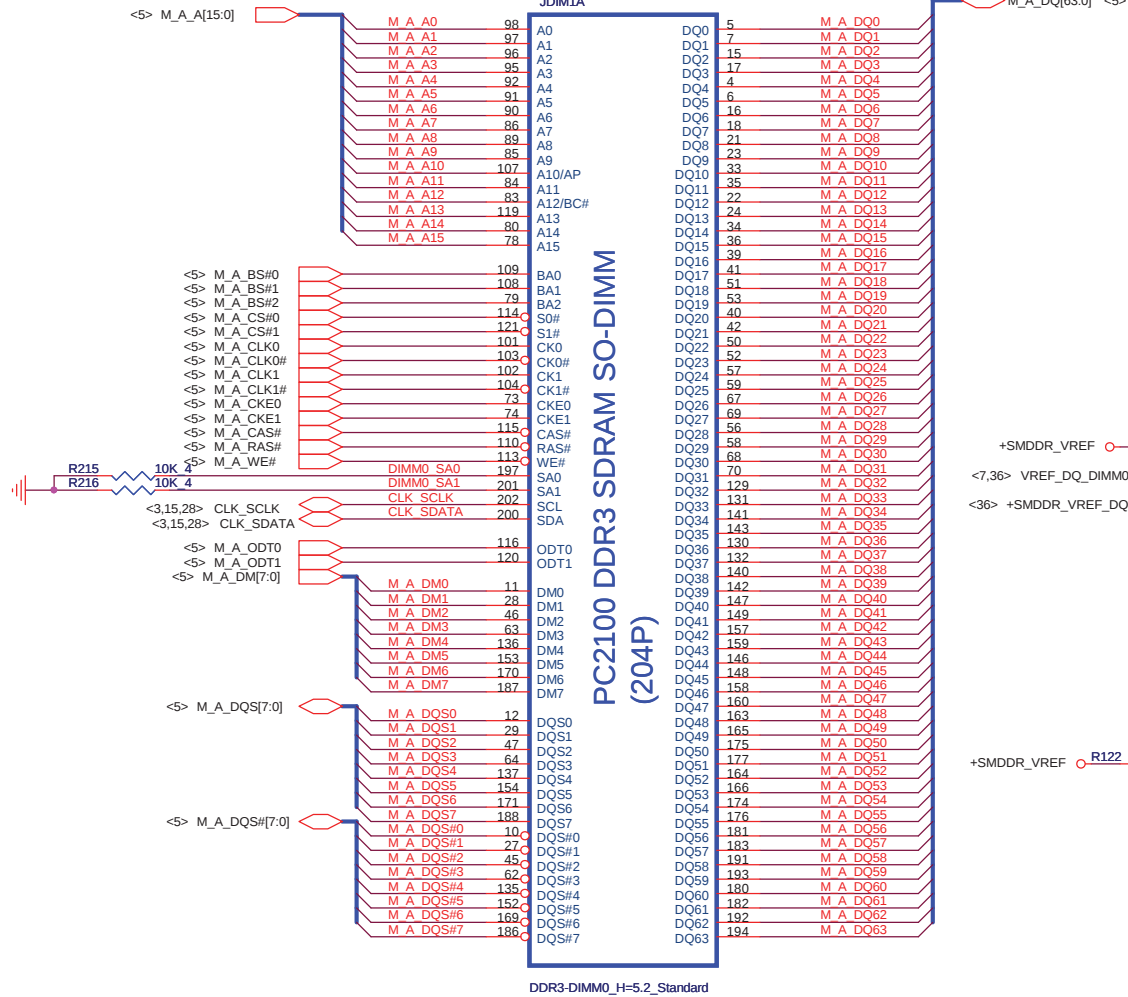
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	IBEX PEAK-M 5/6	1A
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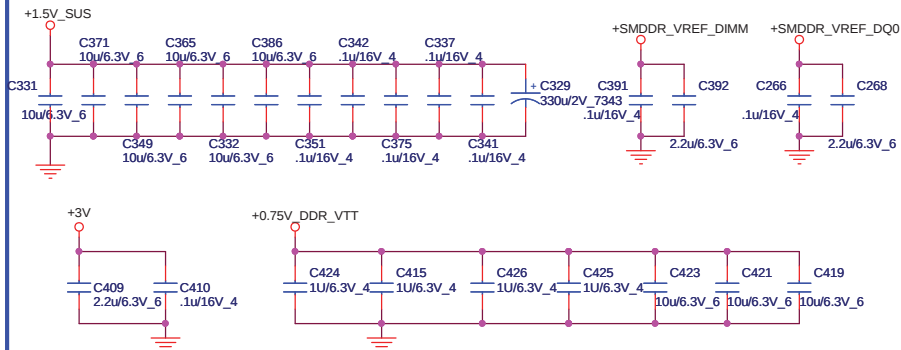
IBEX PEAK-M (GND)

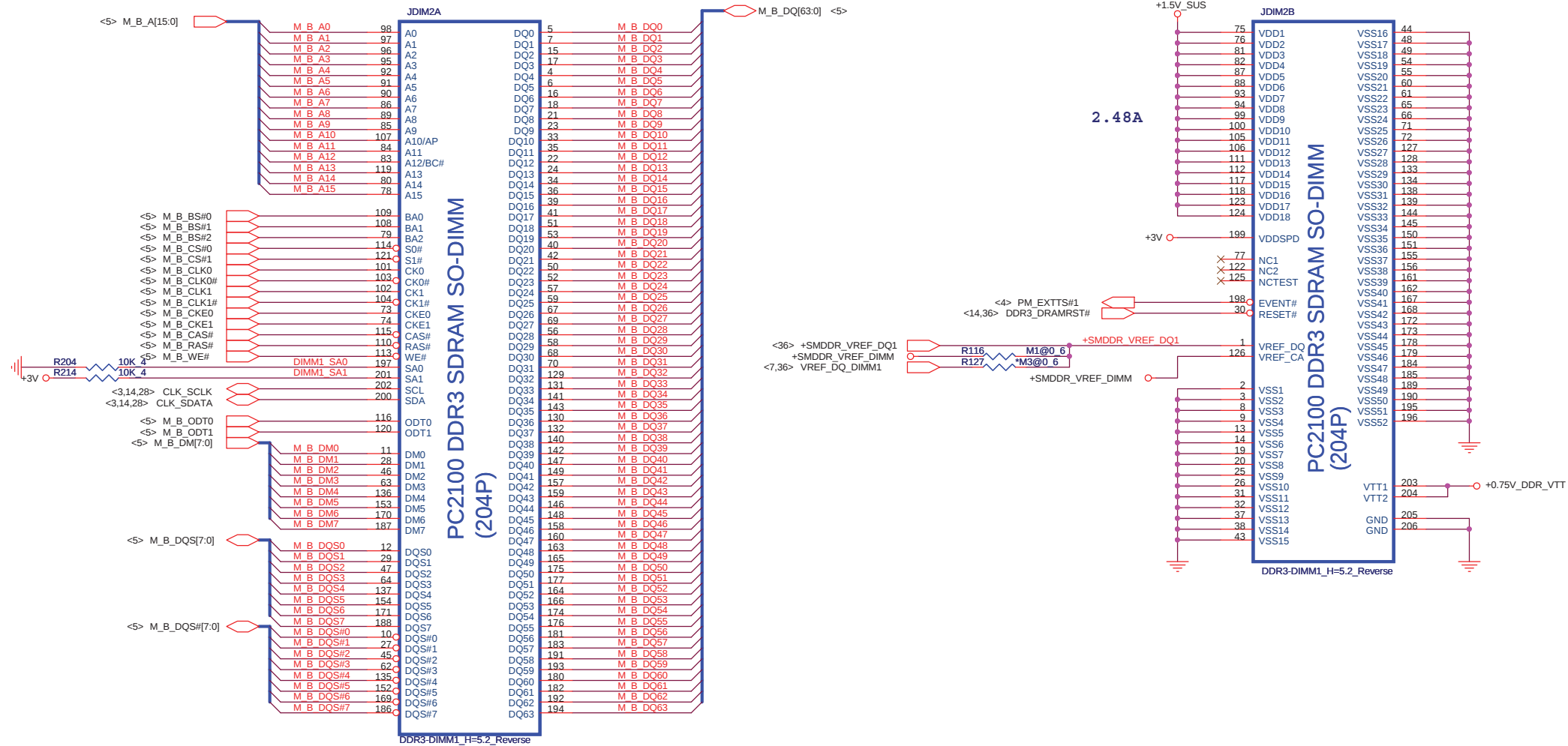


Quanta Computer Inc.
PROJECT : ZR7B

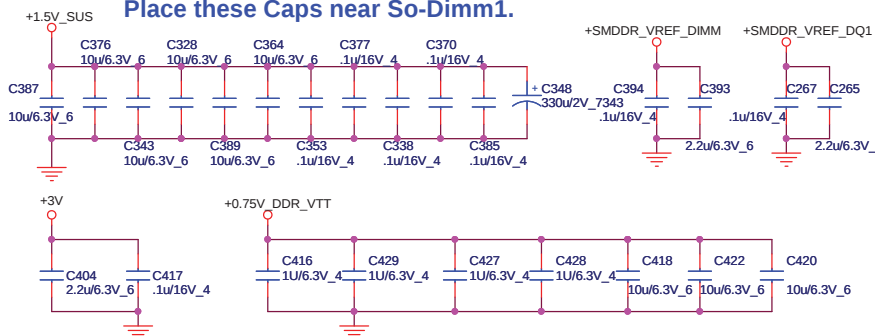


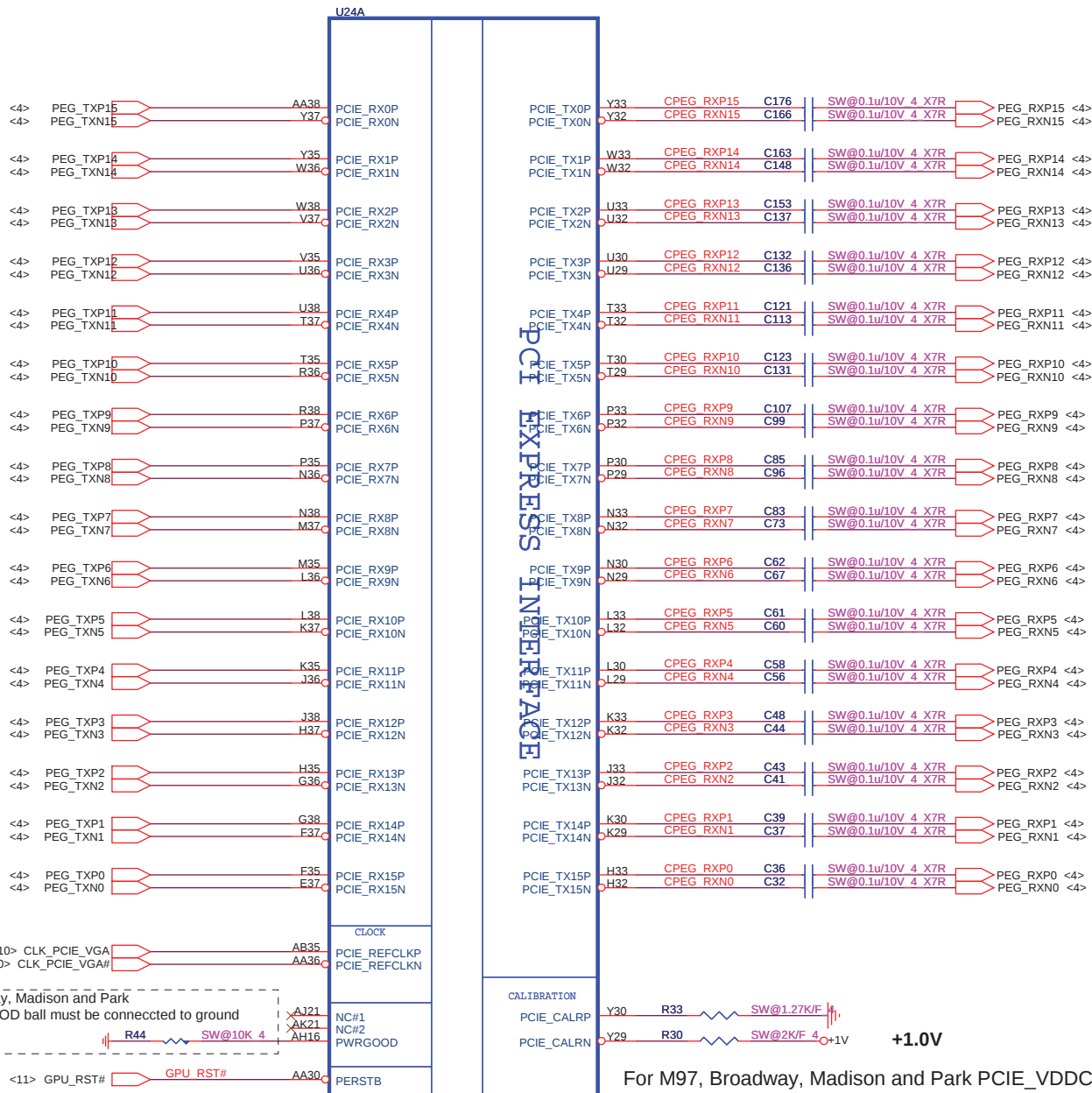
Place these Caps near So-Dimm0.





Place these Caps near So-Dimm1.







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```
1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK
```



<18> VMA_DQ[63..0] VMA_DQ[63..0]
<19> VMA_DM[7..0] VMA_DM[7..0]
<19> VMA_RDQS[7..0] VMA_RDQS[7..0]
<19> VMA_WDQS[7..0] VMA_WDQS[7..0]

<19> VMA_MA[13..0] VMA_MA[13..0]

<18> VMA_BA0 VMA_BA0
<18> VMA_BA1 VMA_BA1
<18> VMA_BA2 VMA_BA2

VMA_DQ0 C37
VMA_DQ1 C38
VMA_DQ2 A35
VMA_DQ3 E34
VMA_DQ4 G32
VMA_DQ5 D33
VMA_DQ6 F32
VMA_DQ7 E32
VMA_DQ8 D31
VMA_DQ9 C30
VMA_DQ10 A30
VMA_DQ11 A30
VMA_DQ12 C28
VMA_DQ13 C28
VMA_DQ14 A28
VMA_DQ15 E28
VMA_DQ16 D27
VMA_DQ17 E26
VMA_DQ18 C26
VMA_DQ19 A26
VMA_DQ20 F24
VMA_DQ21 C24
VMA_DQ22 A24
VMA_DQ23 F24
VMA_DQ24 C22
VMA_DQ25 A22
VMA_DQ26 F22
VMA_DQ27 D21
VMA_DQ28 A20
VMA_DQ29 F20
VMA_DQ30 D19
VMA_DQ31 E18
VMA_DQ32 A18
VMA_DQ33 A18
VMA_DQ34 F18
VMA_DQ35 D17
VMA_DQ36 A16
VMA_DQ37 F16
VMA_DQ38 D15
VMA_DQ39 F14
VMA_DQ40 F14
VMA_DQ41 D13
VMA_DQ42 D12
VMA_DQ43 A12
VMA_DQ44 D11
VMA_DQ45 F10
VMA_DQ46 A10
VMA_DQ47 C10
VMA_DQ48 G13
VMA_DQ49 H13
VMA_DQ50 J13
VMA_DQ51 H11
VMA_DQ52 G10
VMA_DQ53 G8
VMA_DQ54 K9
VMA_DQ55 K10
VMA_DQ56 G9
VMA_DQ57 A8
VMA_DQ58 F8
VMA_DQ59 A6
VMA_DQ60 A6
VMA_DQ61 C6
VMA_DQ62 A5
VMA_DQ63 A5

U24C

DDR2

DDR3/DDR5

DDR3

MAA0_0MAA_0

MAA0_1MAA_1

MAA0_2MAA_2

MAA0_3MAA_3

MAA0_4MAA_4

MAA0_5MAA_5

MAA0_6MAA_6

MAA0_7MAA_7

MAA1_0MAA_8

MAA1_1MAA_9

MAA1_2MAA_10

MAA1_3MAA_11

MAA1_4MAA_12

MAA1_5MAA_13

MAA1_6MAA_14

MAA1_7MAA_15

MAA1_8MAA_16

MAA1_9MAA_17

MAA1_10MAA_18

MAA1_11MAA_19

MAA1_12MAA_20

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MAA1_14MAA_22

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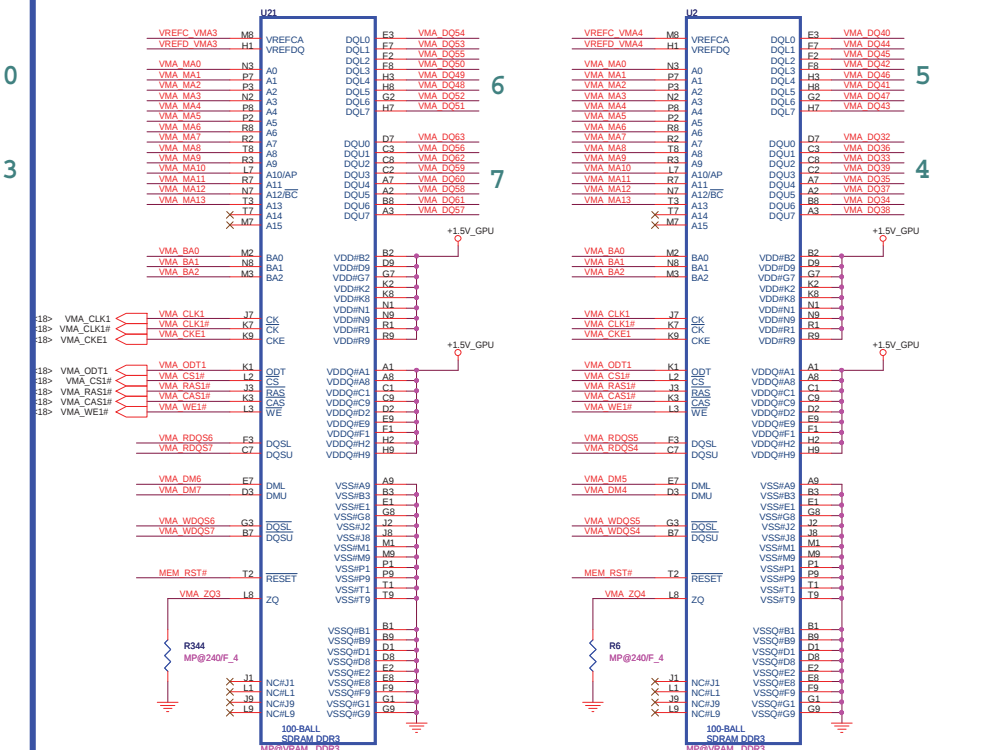
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MAA1_232MAA_240

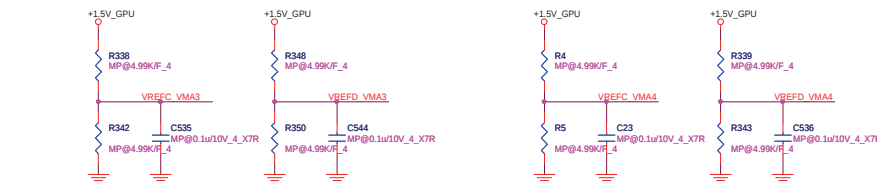
MAA1_233MAA_241

MAA1_234MAA_2

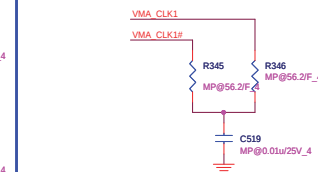
Park, M92M Use Channel B Memory Interface Only



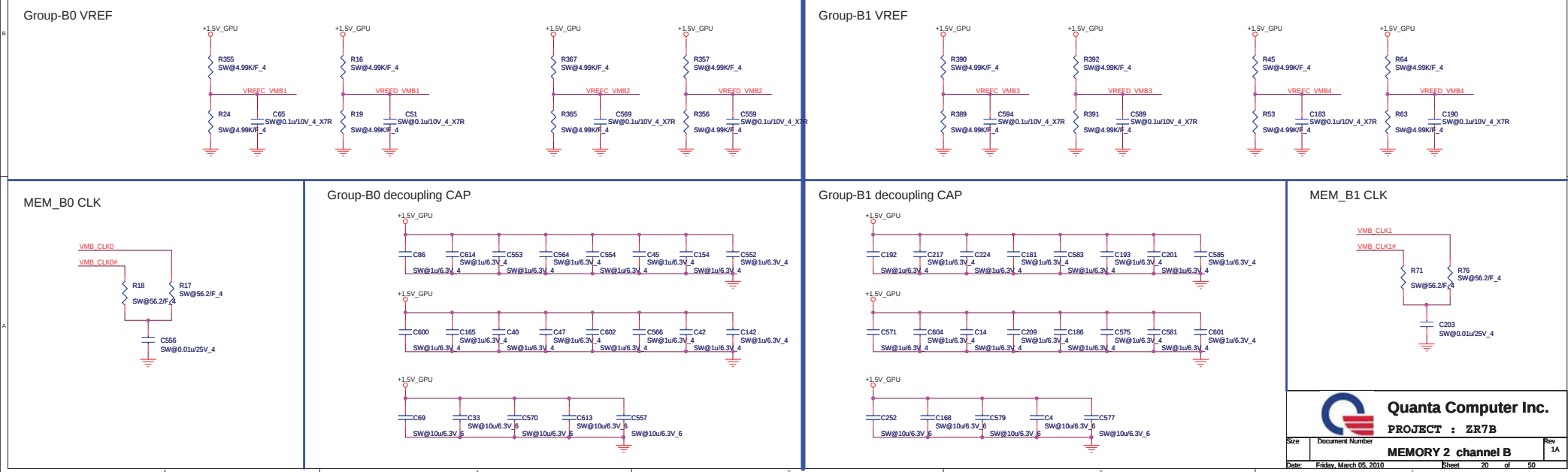
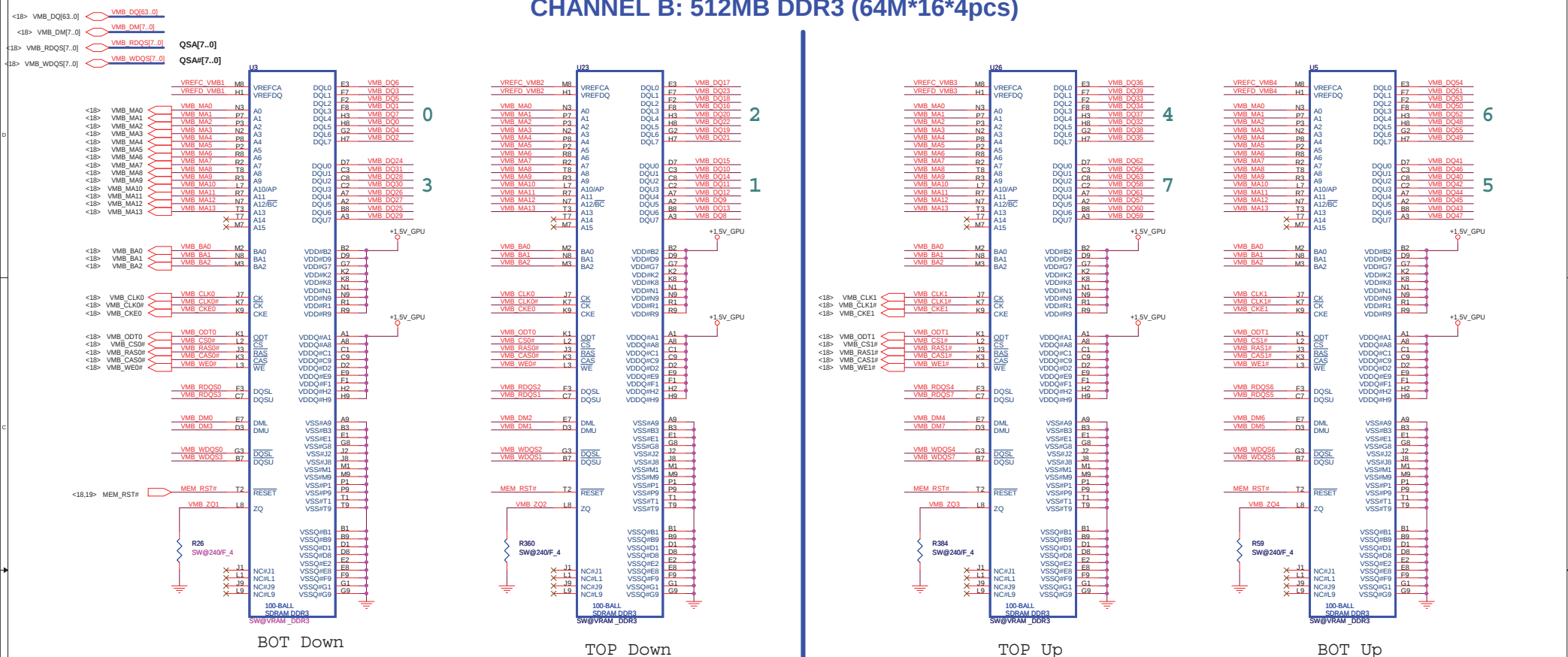
TOP Right

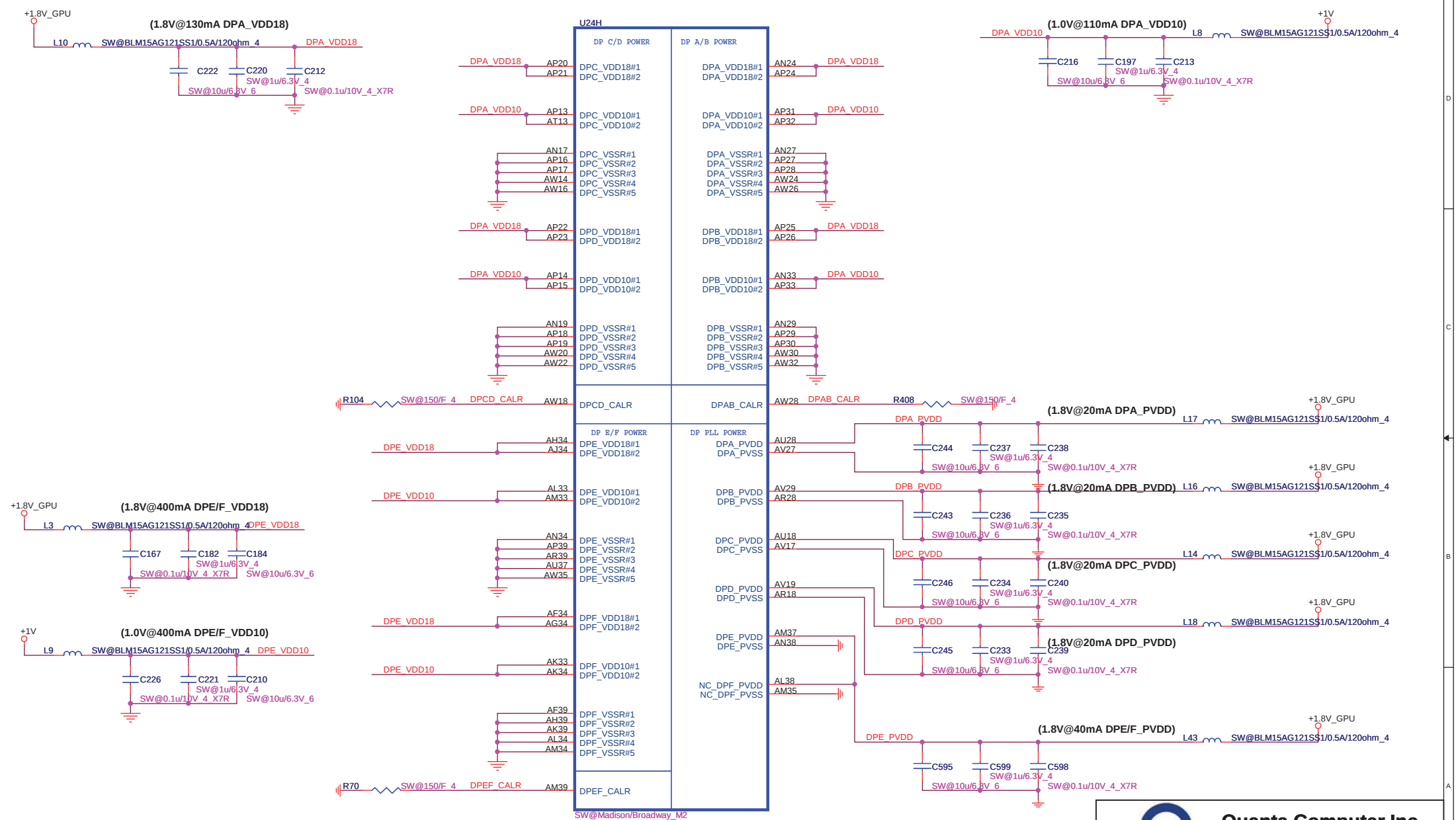


MEM A1 CLK



CHANNEL B: 512MB DDR3 (64M*16*4pcs)



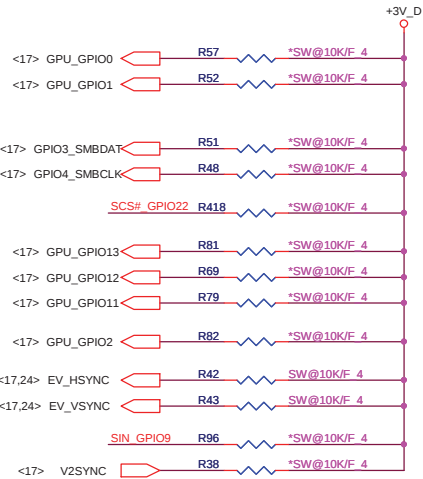




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	Madison/Broadway (DP_PWR/GND)	1A
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PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

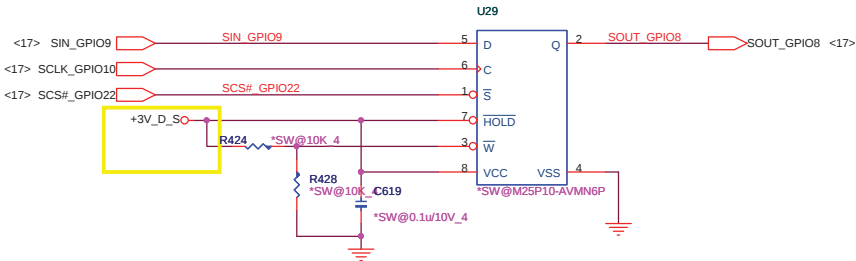
ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

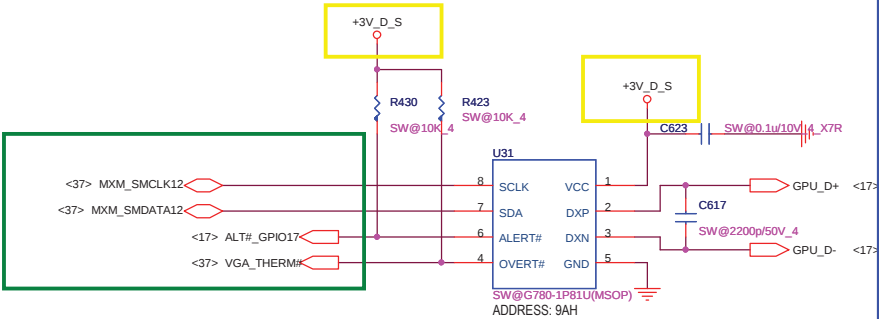
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM



Thermal Sensor

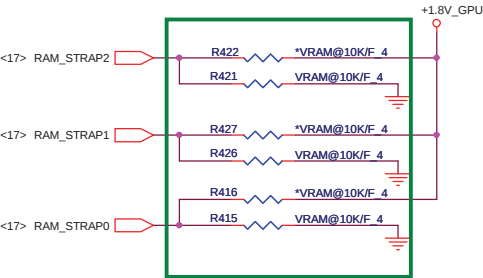
NS	none
WINDBOND	AL83L771K02
GMT	AL000780003



DDR3 Memory Aperture size

DDR3 Memory Aperture size

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	512MB	1	1	0
			1GB	1	0	0
			2GB	1	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	512MB			
	K4W2G1646B-HC12	AKD5MGGT500	1GB	0	0	0
AMD	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1
	23EY2387MA12-SZ	AKD5LGGT700	1GB	0	1	0



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

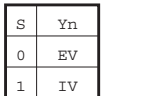


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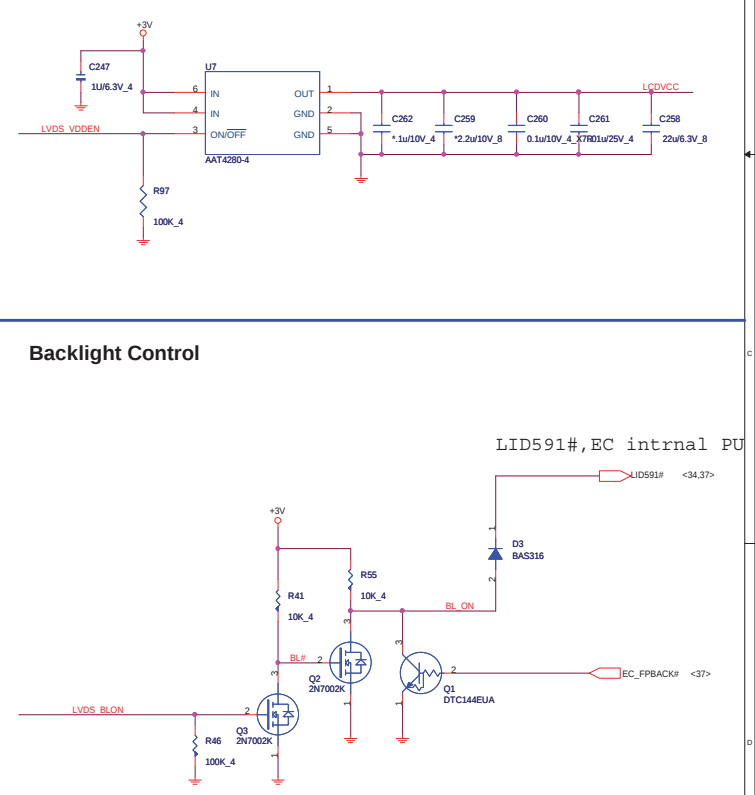
Size	Document Number	Rev
	Strip/Thermal	1A
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IV@
SW@[illegible]

LVDS

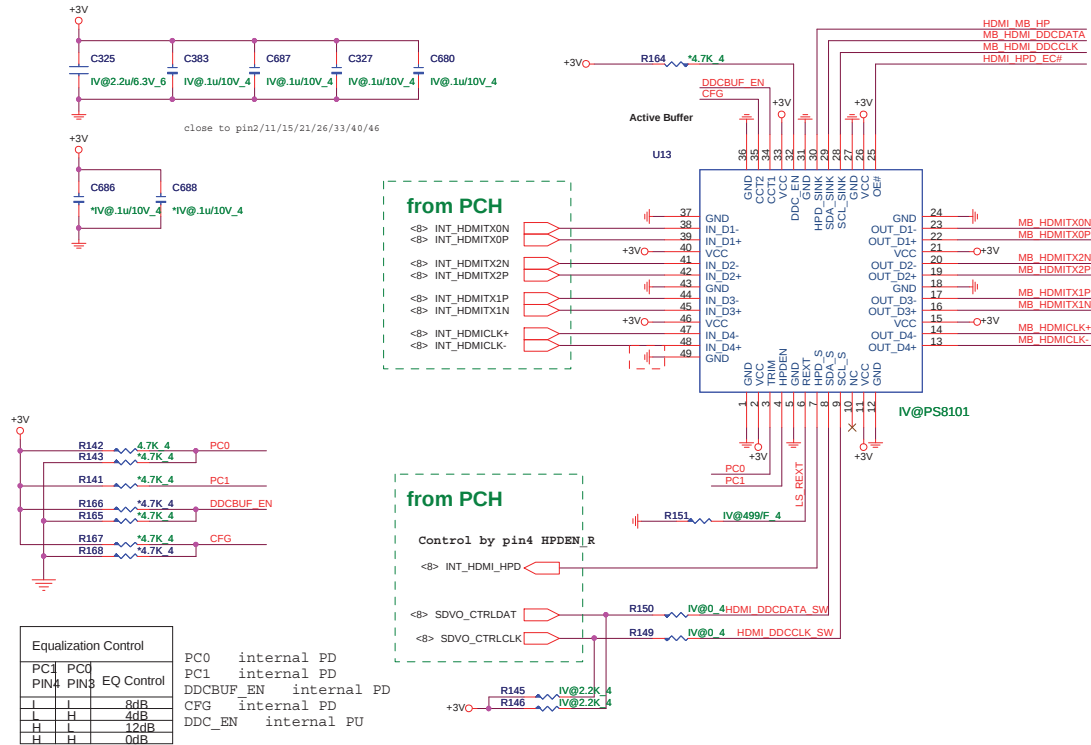


Backlight Control

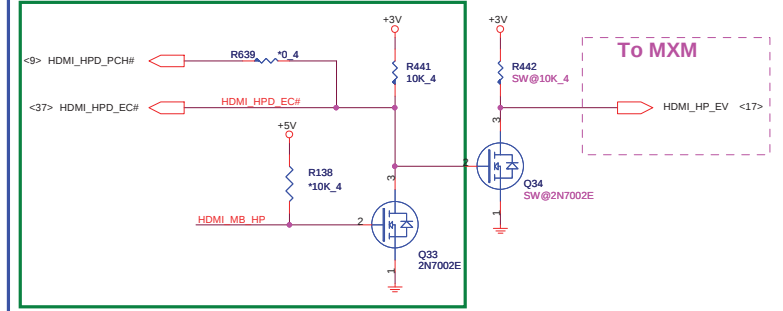


I@ HDMI LEVEL SHIFTER

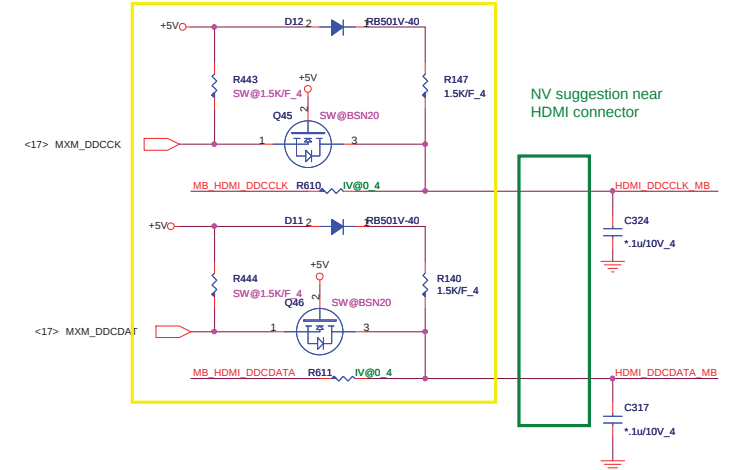
IV@
SW@
SP@



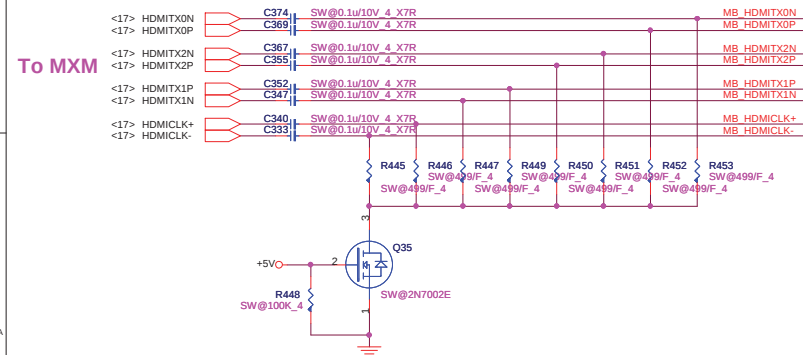
SW@HDMI-detect



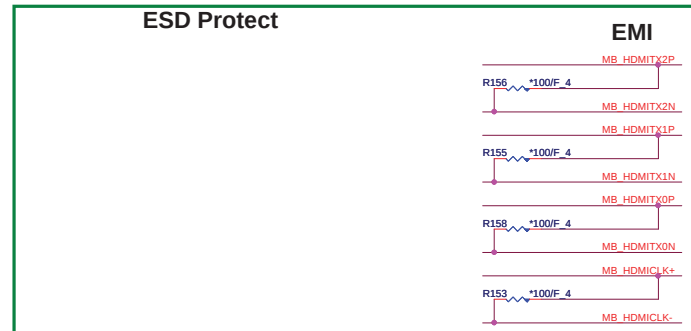
I2C



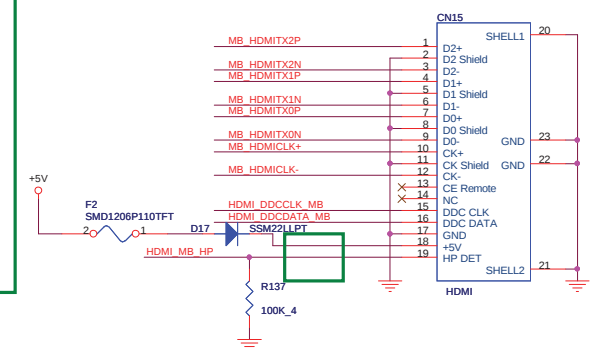
Switchable Graphic HDMI source



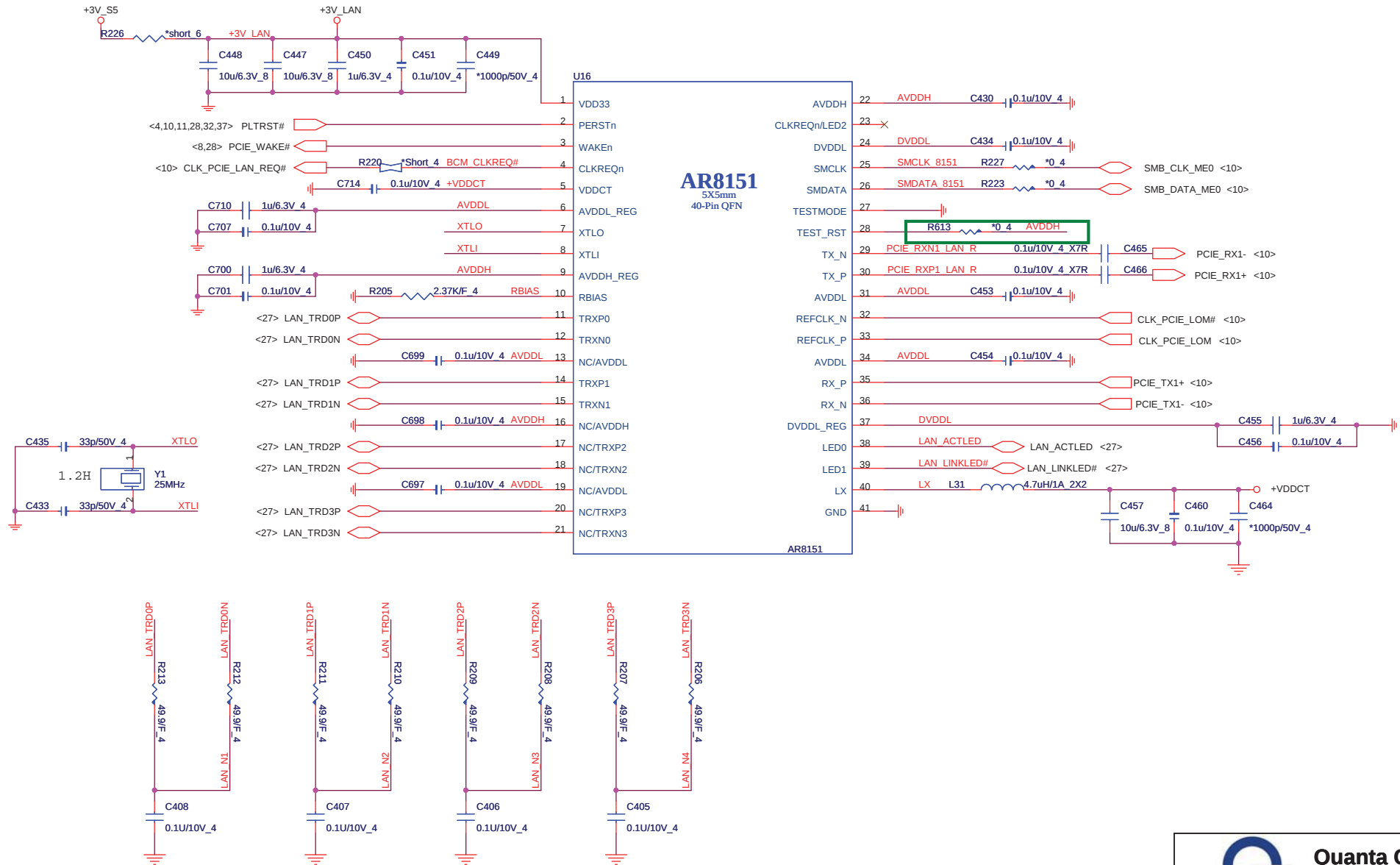
ESD Protect

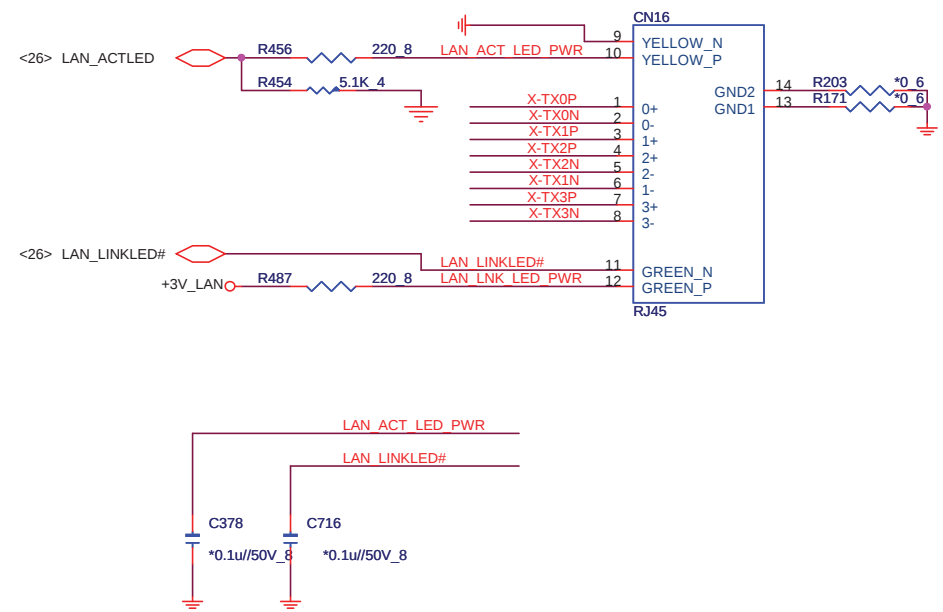
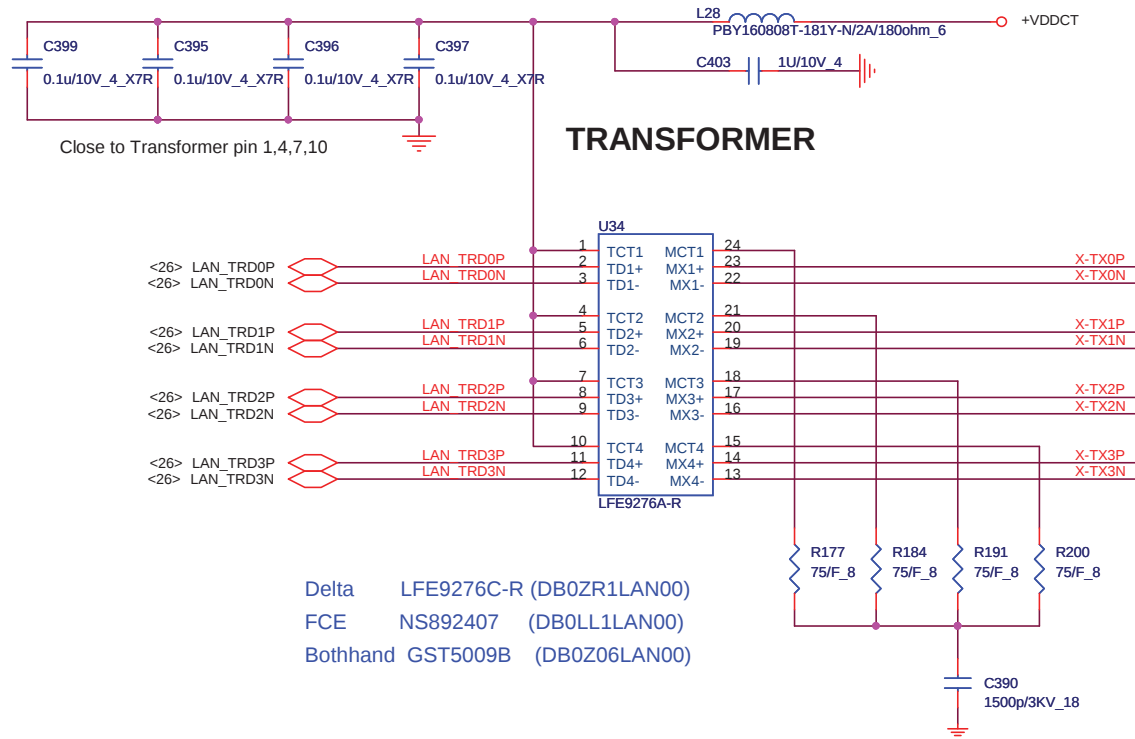


HDMI connector

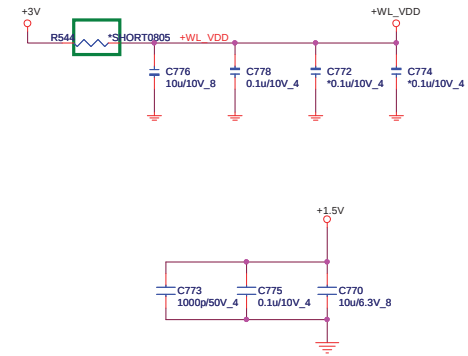


Giga-LAN AR8151

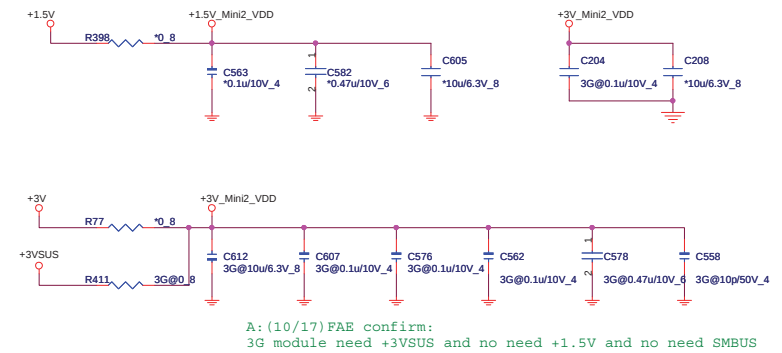
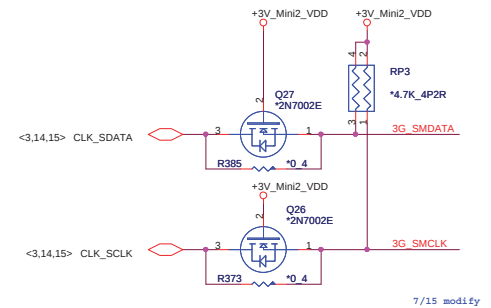
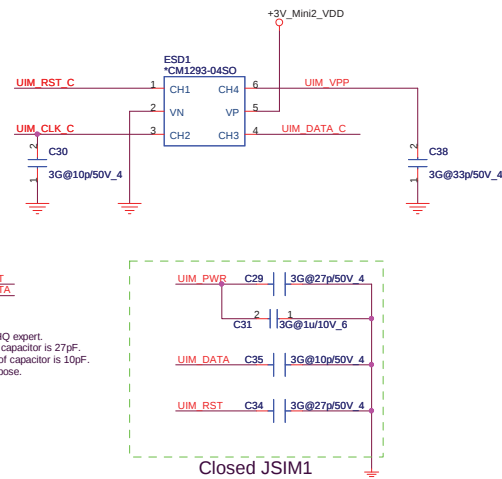




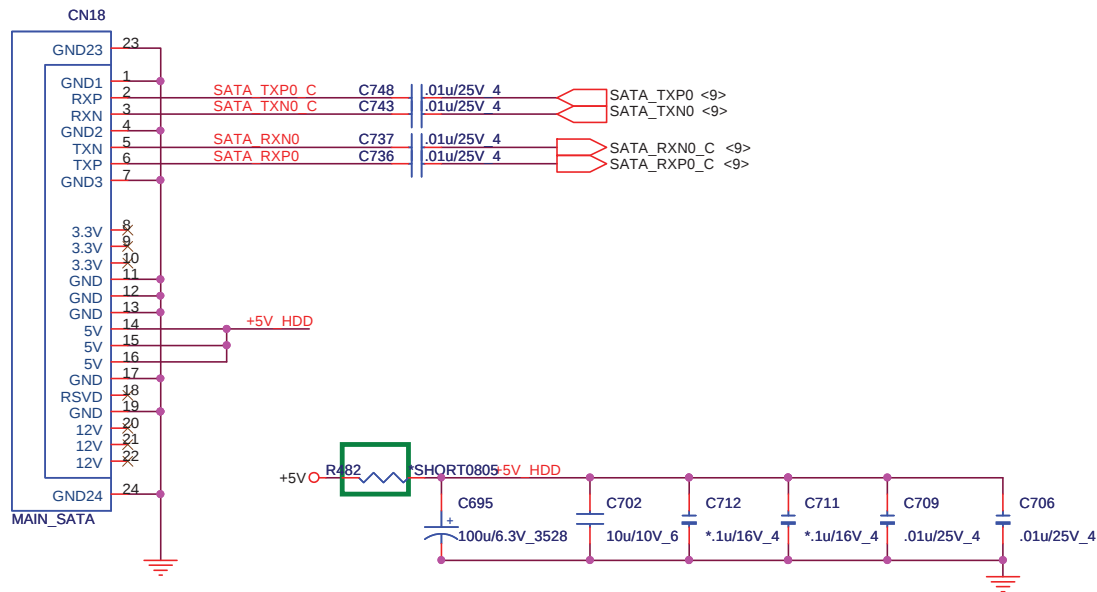
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



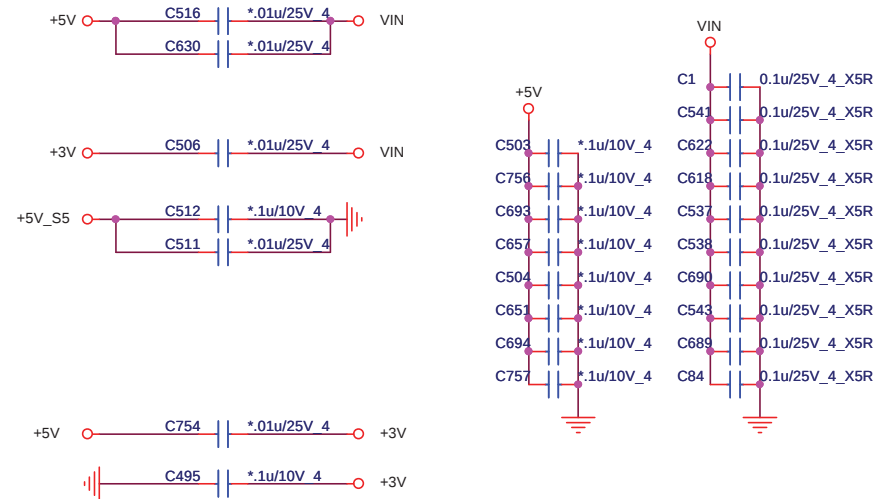
The diagram illustrates the PCB layout for the H=7.0mm module, showing the connection of the CN12 connector to the board. The layout includes power planes, signal traces, and component footprints. Key components include the CN12 connector, various resistors (R397, R394, R393, R396, R398, R368), and LEDs (3G MINI LED#, RF LED#, 3G_EN). The layout is labeled with "H=7.0mm" and "Active Low". The connector pins are numbered 1 to 51, and the board components are labeled with their respective values and footprints.

[illegible]

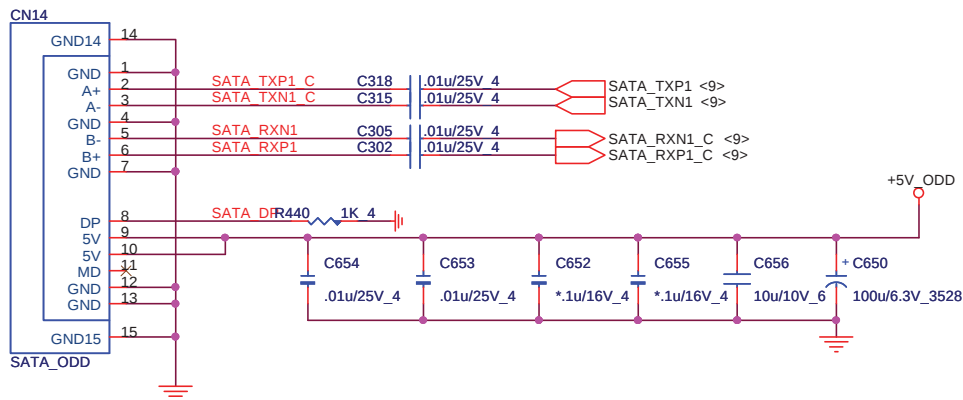
MAIN SATA HDD



EE RETURN-PATH CAPACITORS

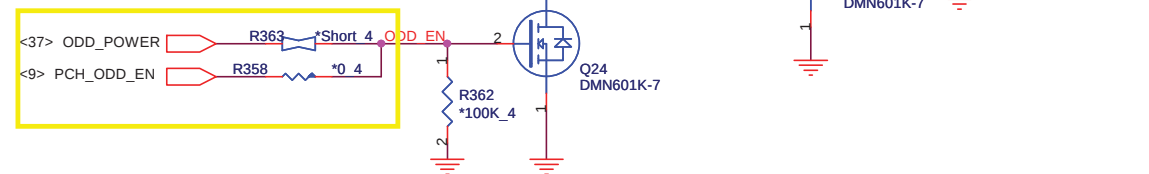


ODD (SATA)



ODD POWER(ODD)

Connect to PCH(GPIO21) pin Y9 and EC pin28 (GPIO53)



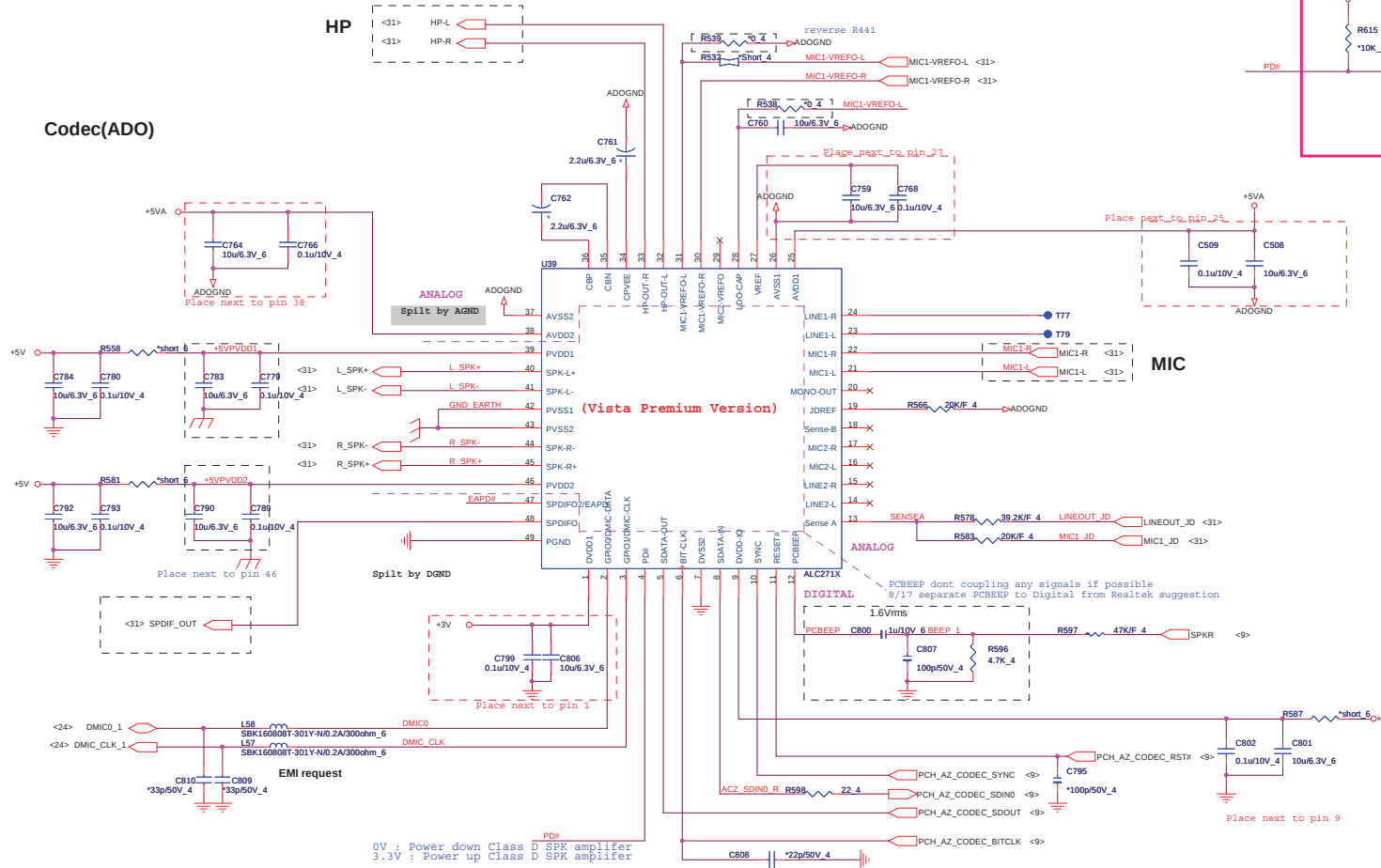
Quanta Computer Inc.

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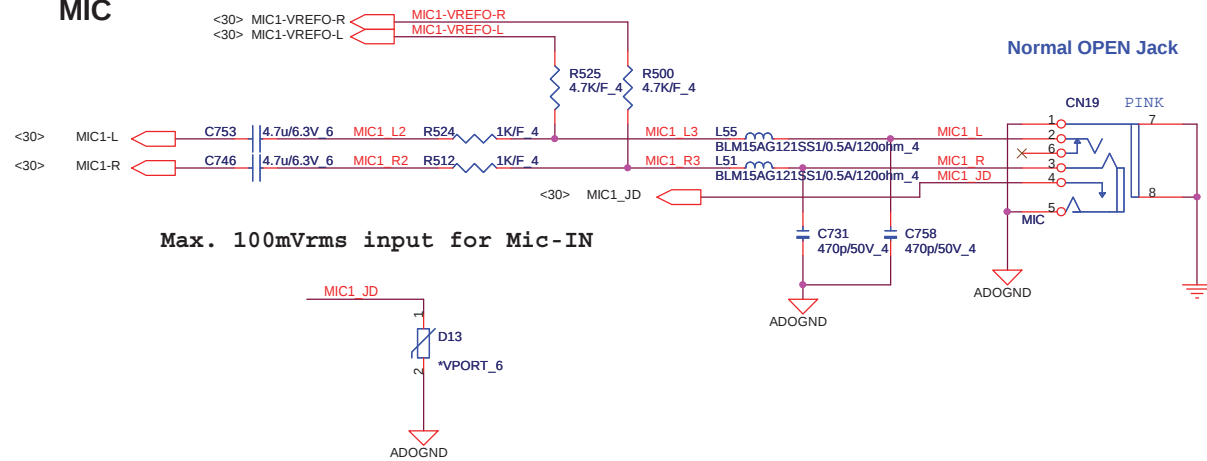
Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A

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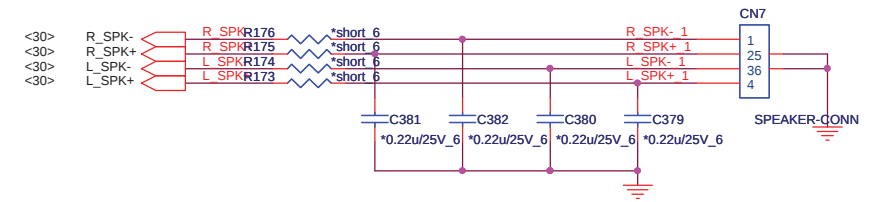
Codec(ADO)



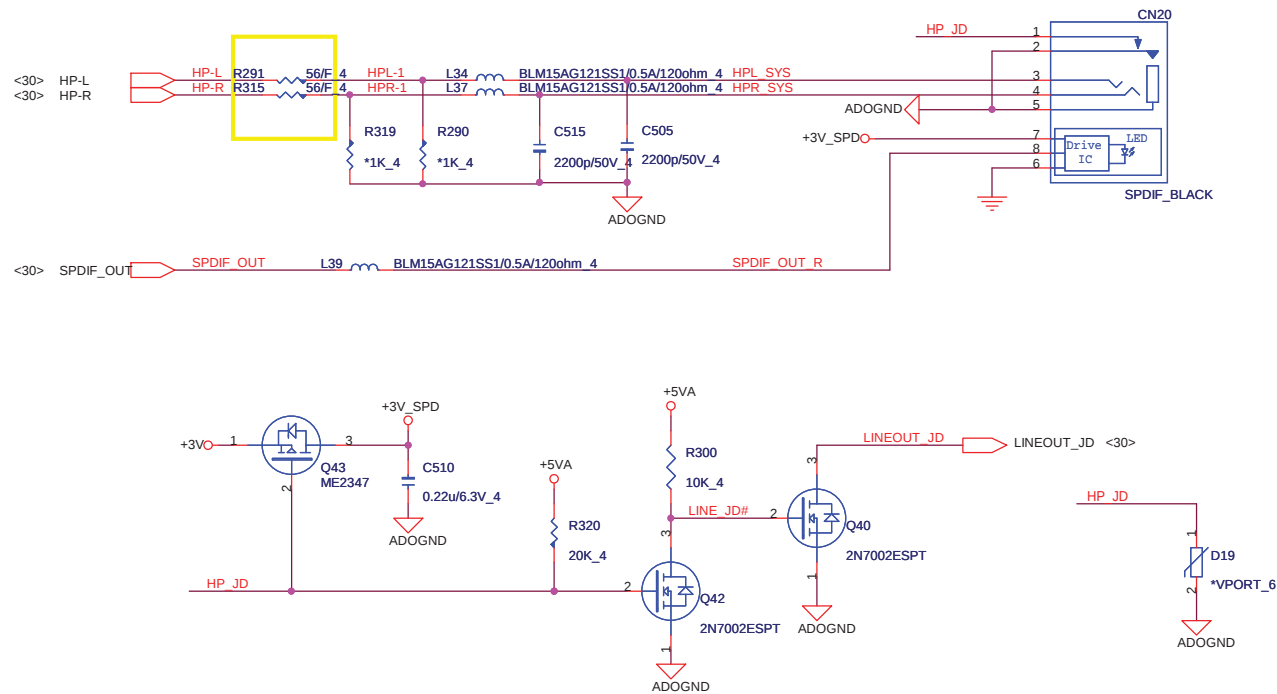
MIC



Internal Speaker

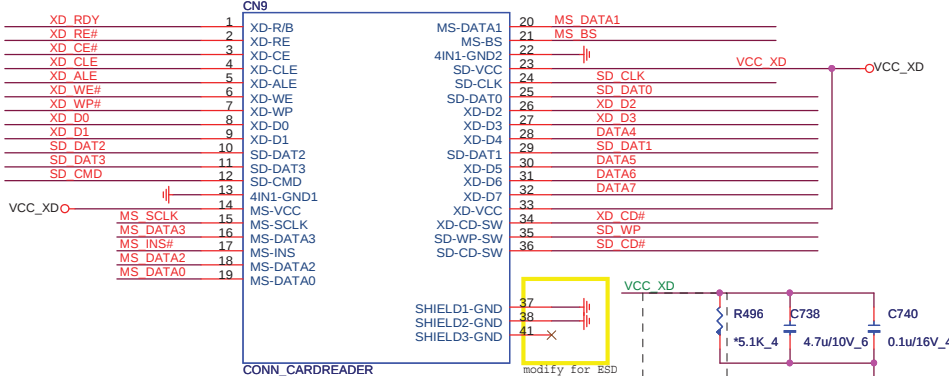


HP/SPDIF

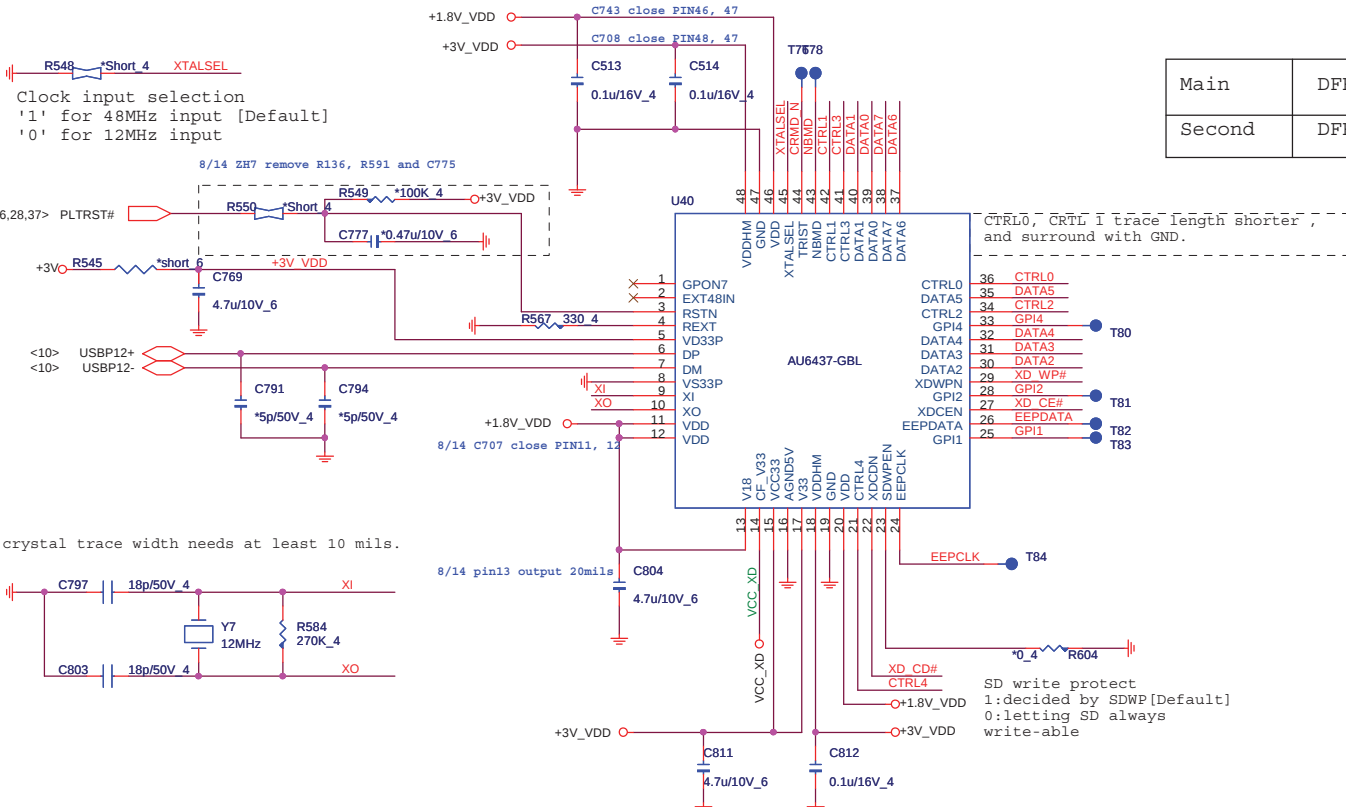


CARD READER Controller

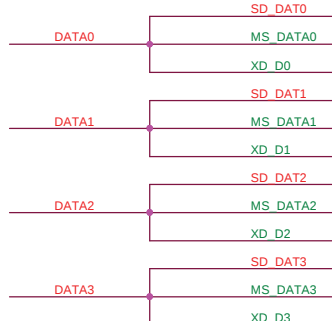
4 IN 1 CARD READER (MMC)



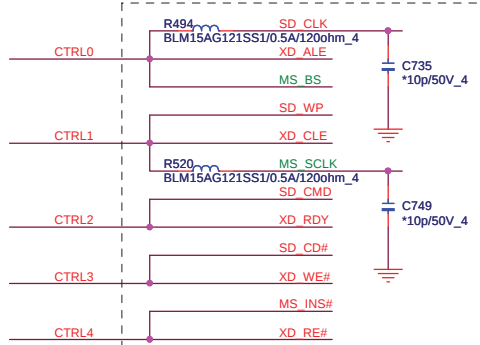
Close to CN14 pin 14 & pin23
4.7u CAP close to pin23



Main	DFHD36MS006
Second	DFHD36MS012



Close to connector

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AU6433 CardReader

Size

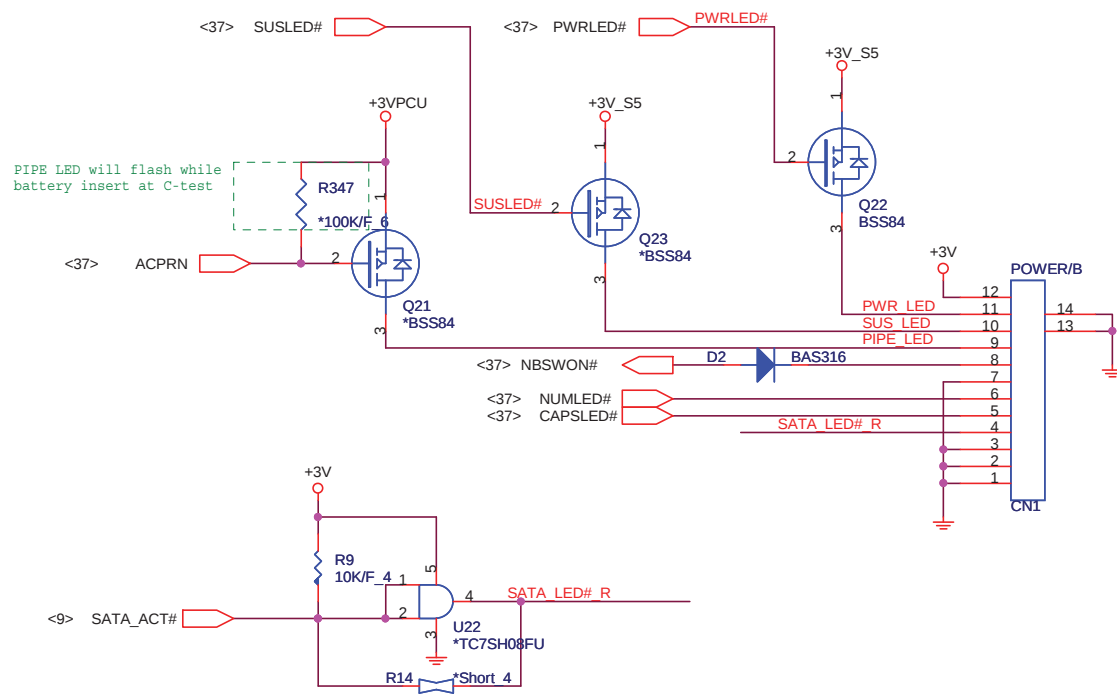
Document Number

Rev

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POWER BOARD CONN(UIF)

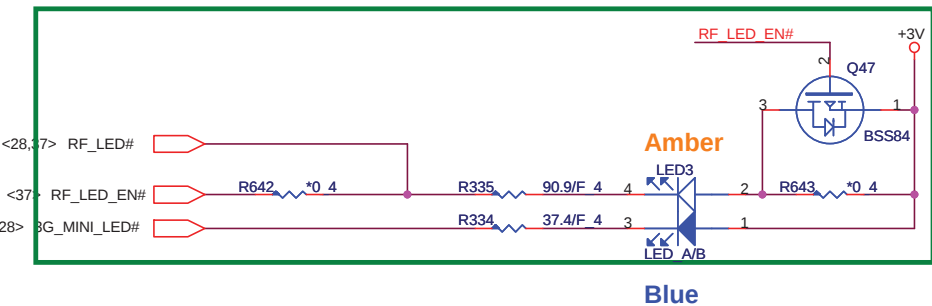
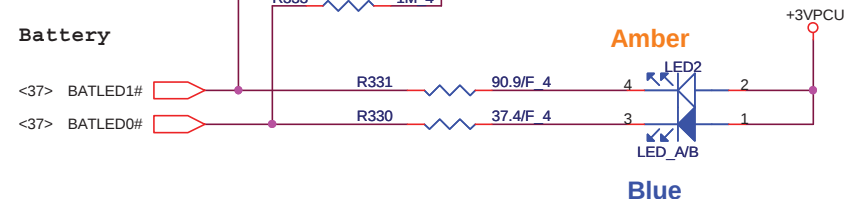


LED

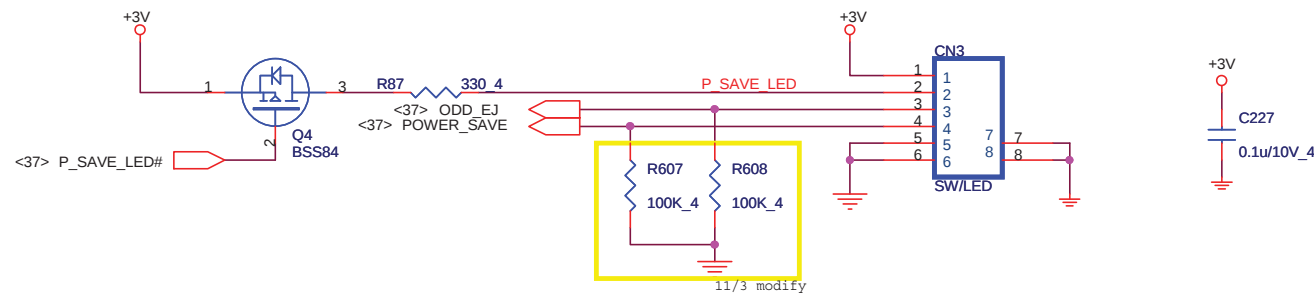
POWER



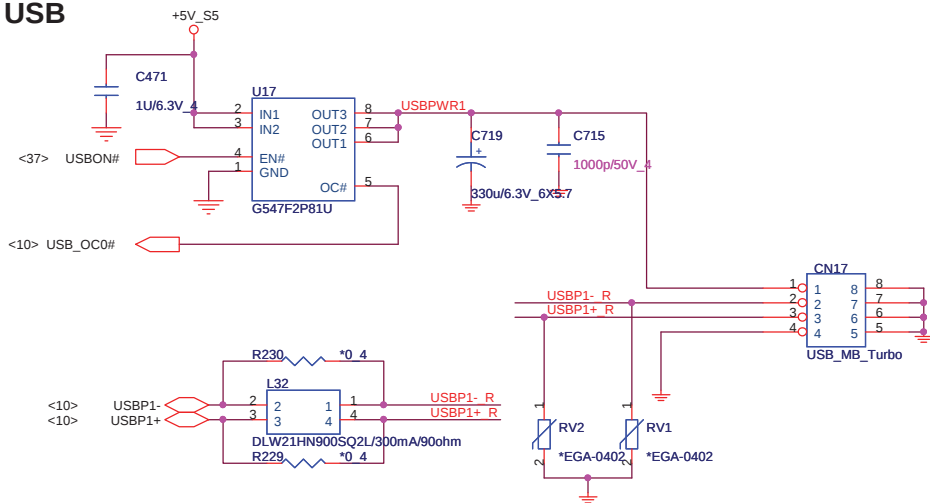
Battery



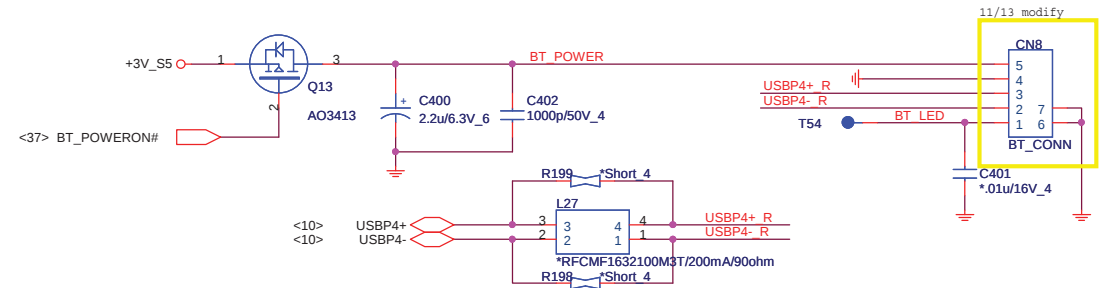
SW /B



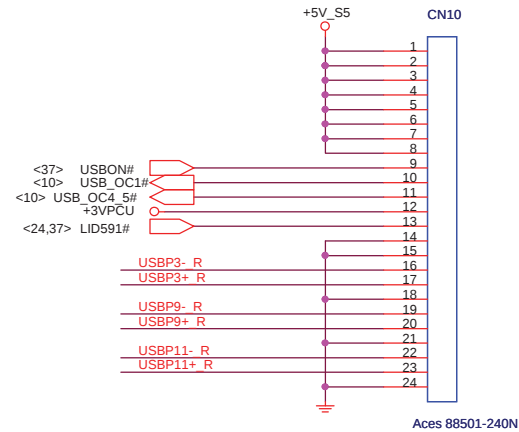
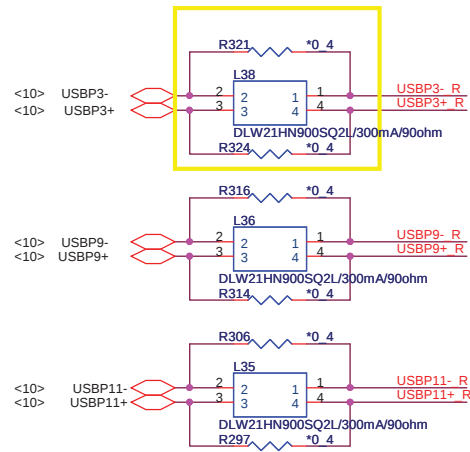
USB



BLUETOOTH CONNECTOR



USB/B



R230, R229, R321, R324, R316, R314, R306, R297

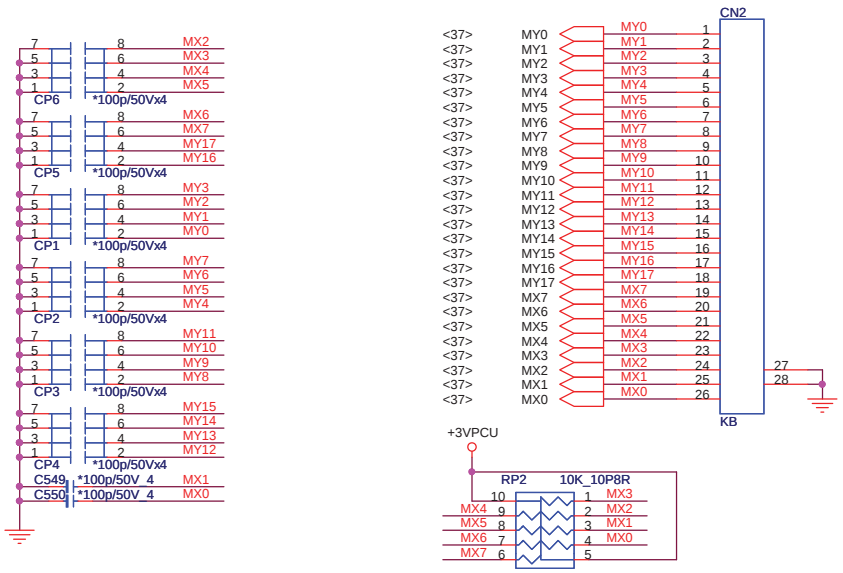


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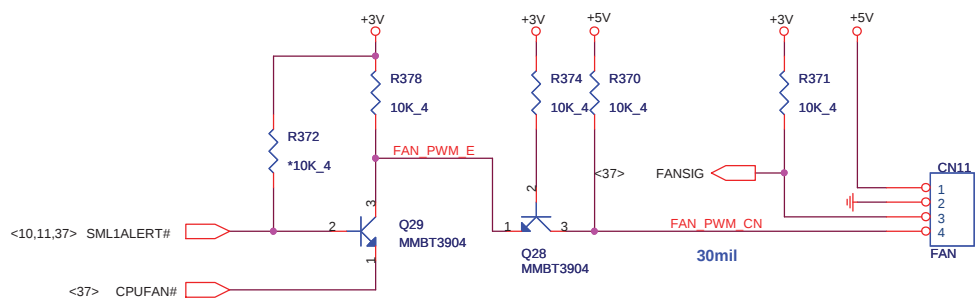
PROJECT : ZR7B

Size	Document Number	Rev
	USB/ BT	1A

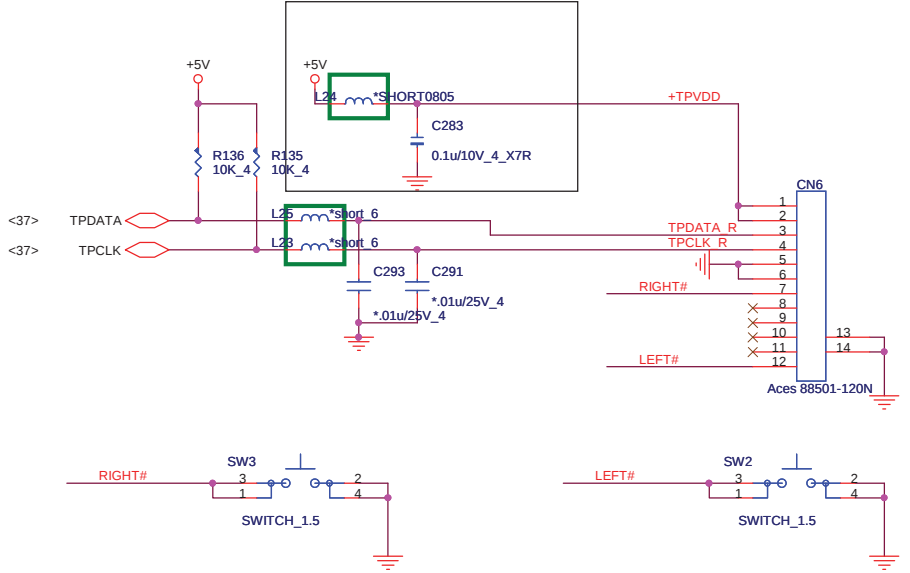
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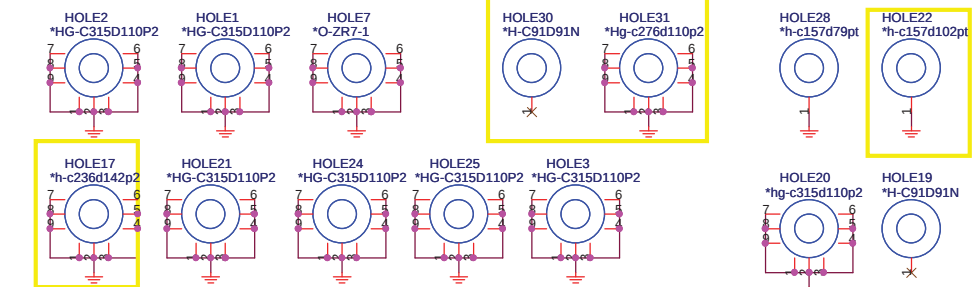
CPU FAN



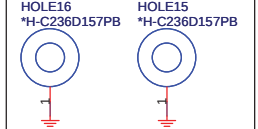
TOUCHPAD & Switch CONN.



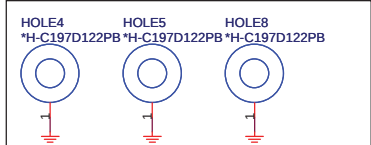
H-C157D63PT



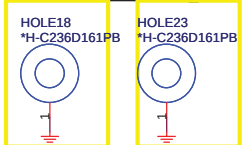
H-C236D157PB



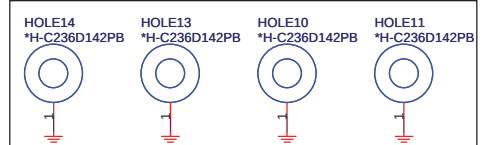
H-C197D122PB



h-c236d118p2



H-C236D142PB

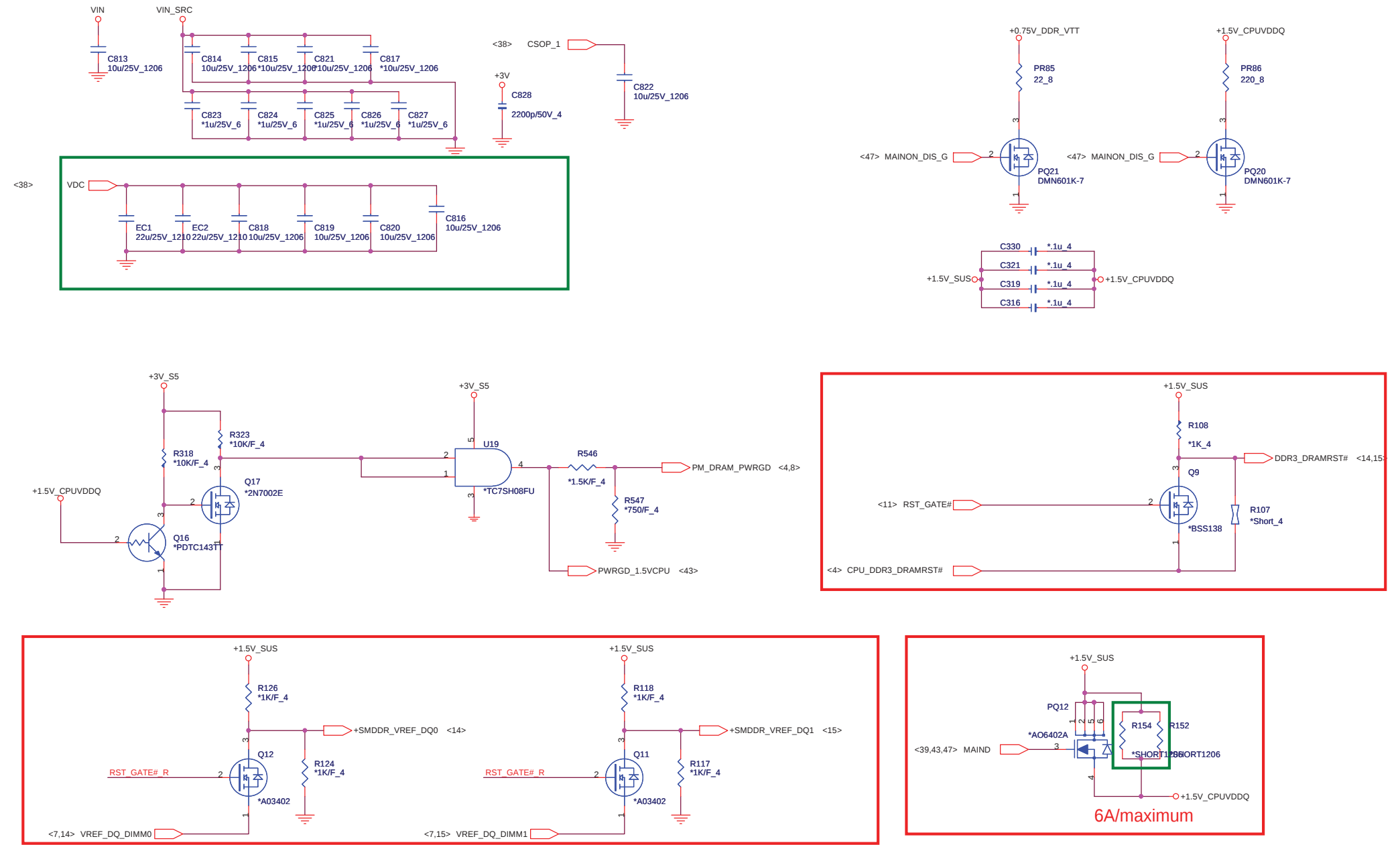




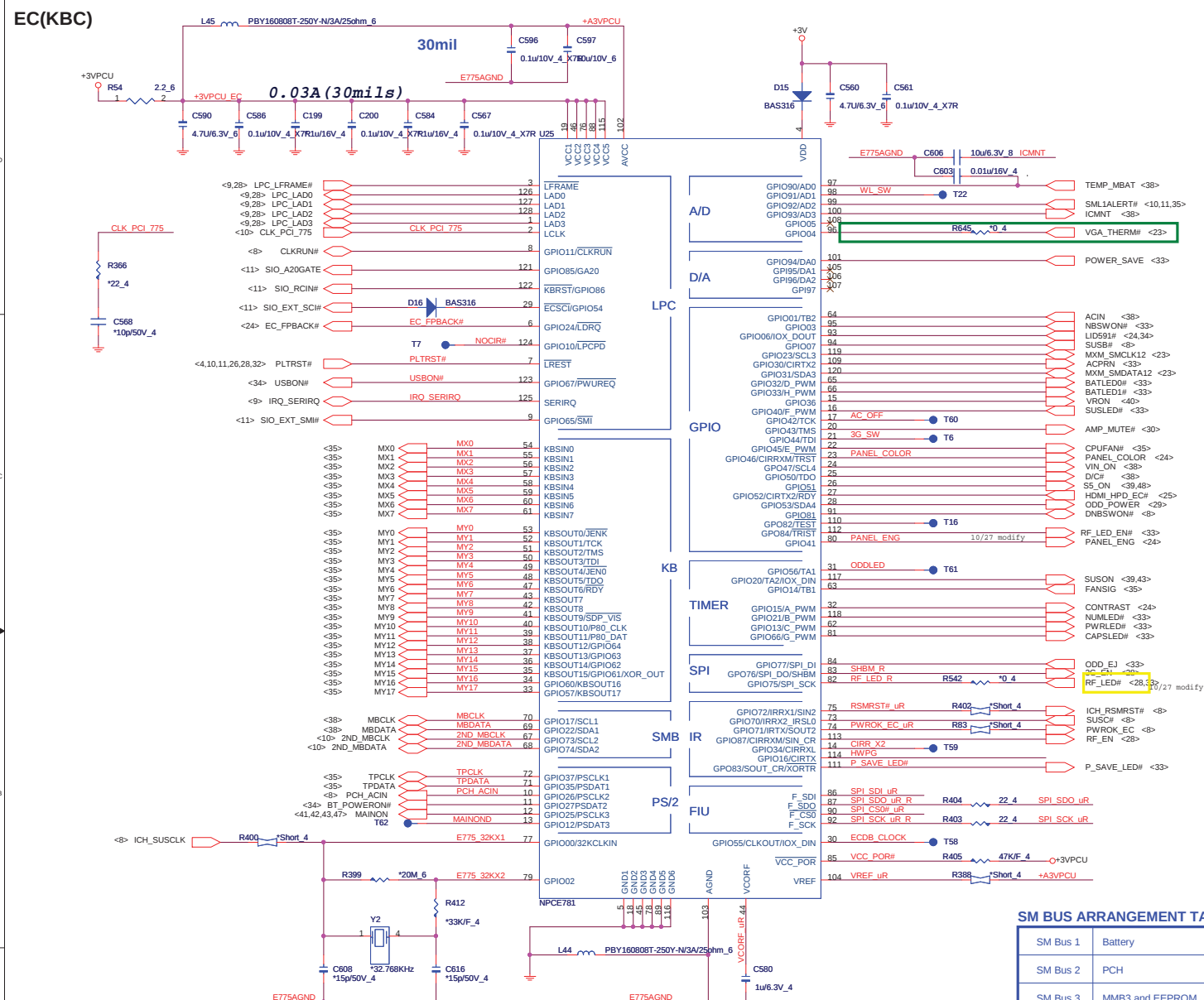
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EMI decoupling

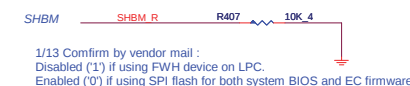


EC(KBC)

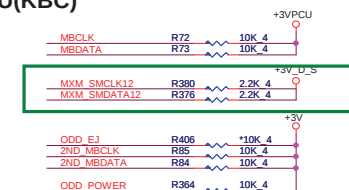


I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS



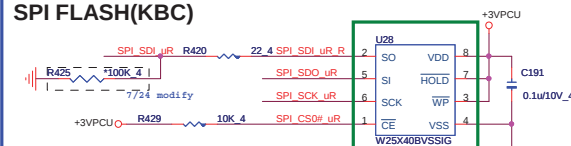
SM BUS PU(KBC)



ACER ID(KBC)

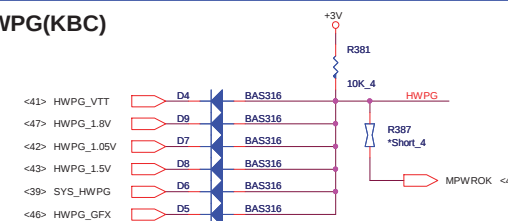


SPI FLASH(KBC)

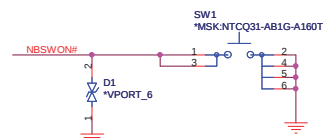


1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or fa

HWPG(KBC)

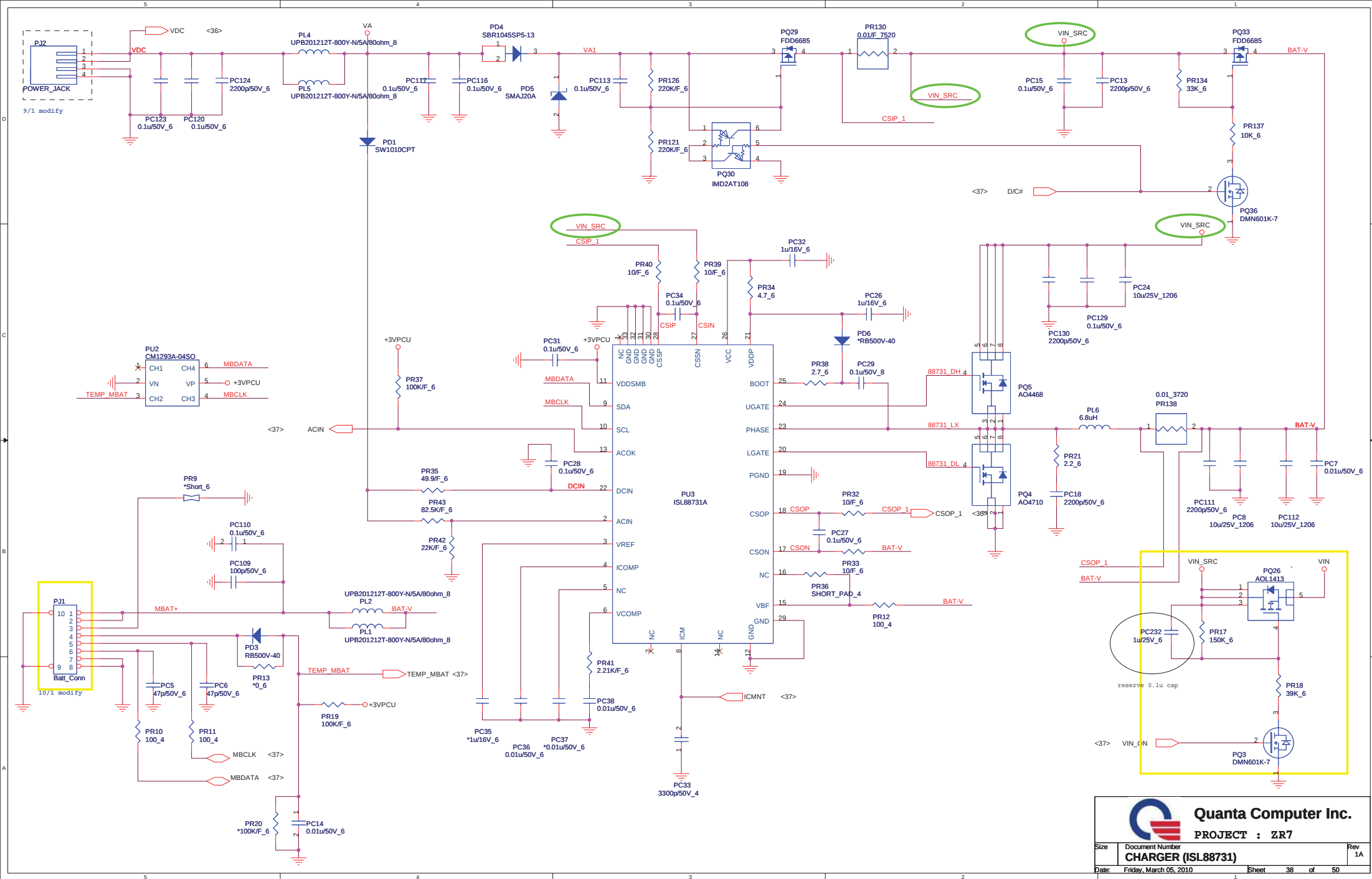


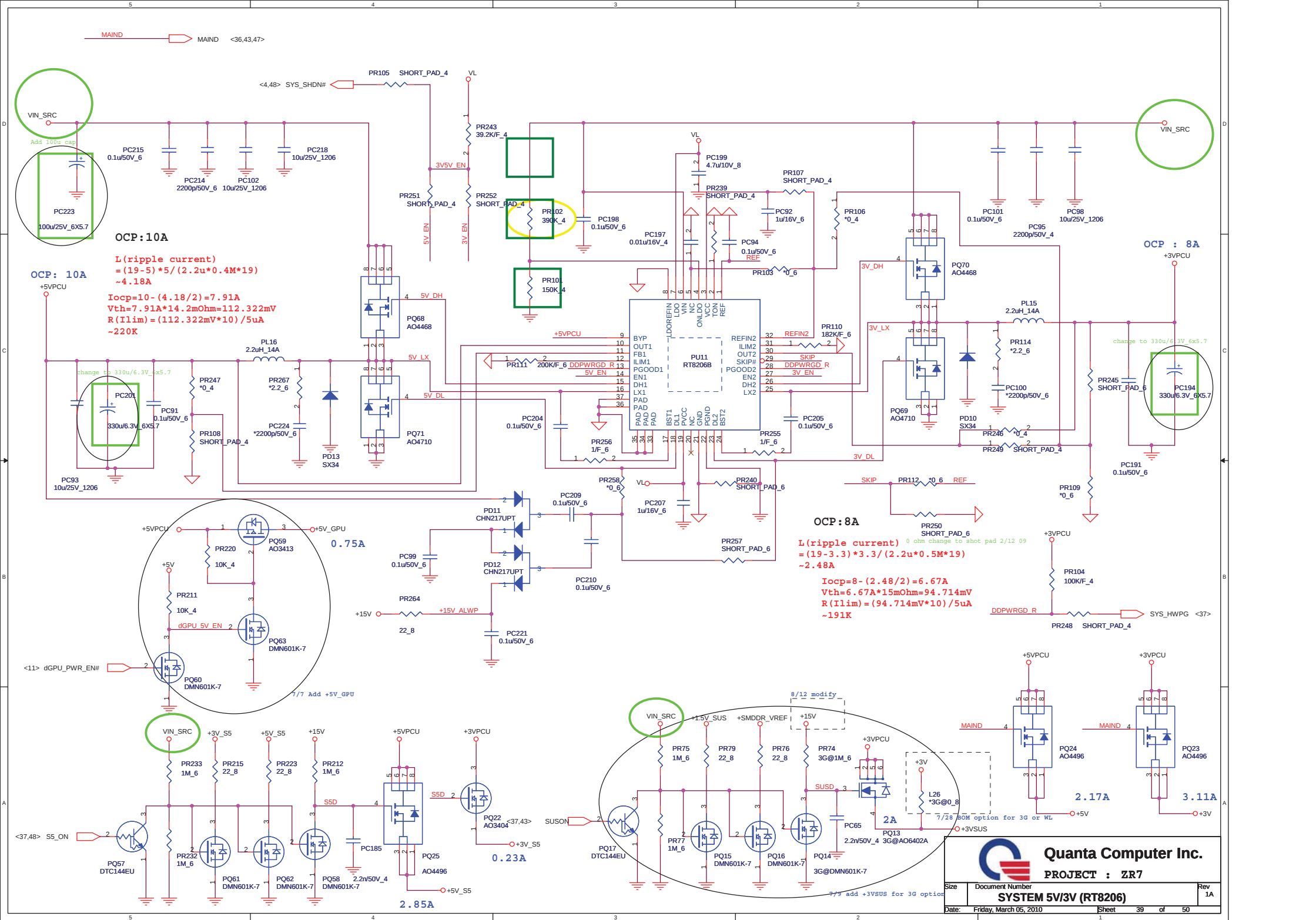
POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

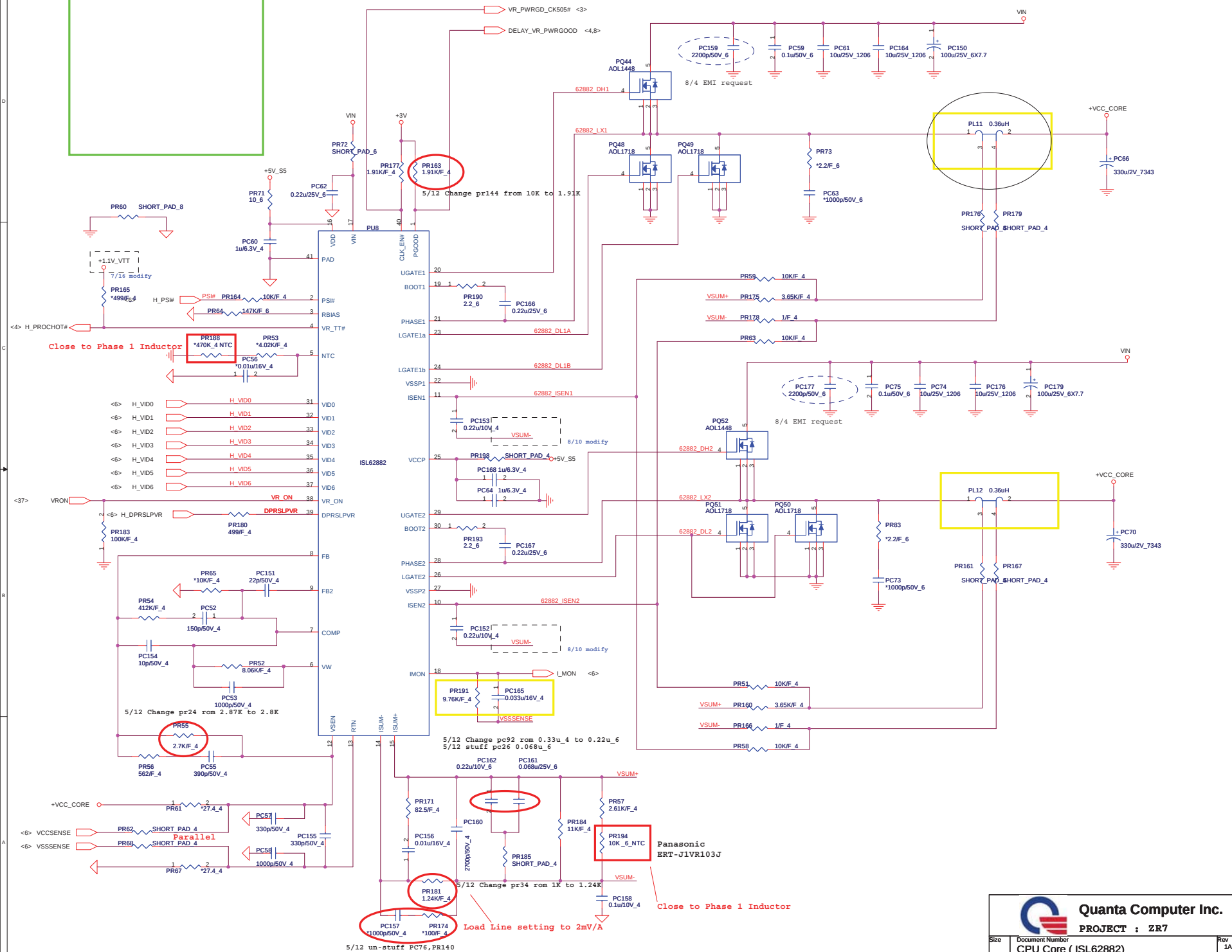




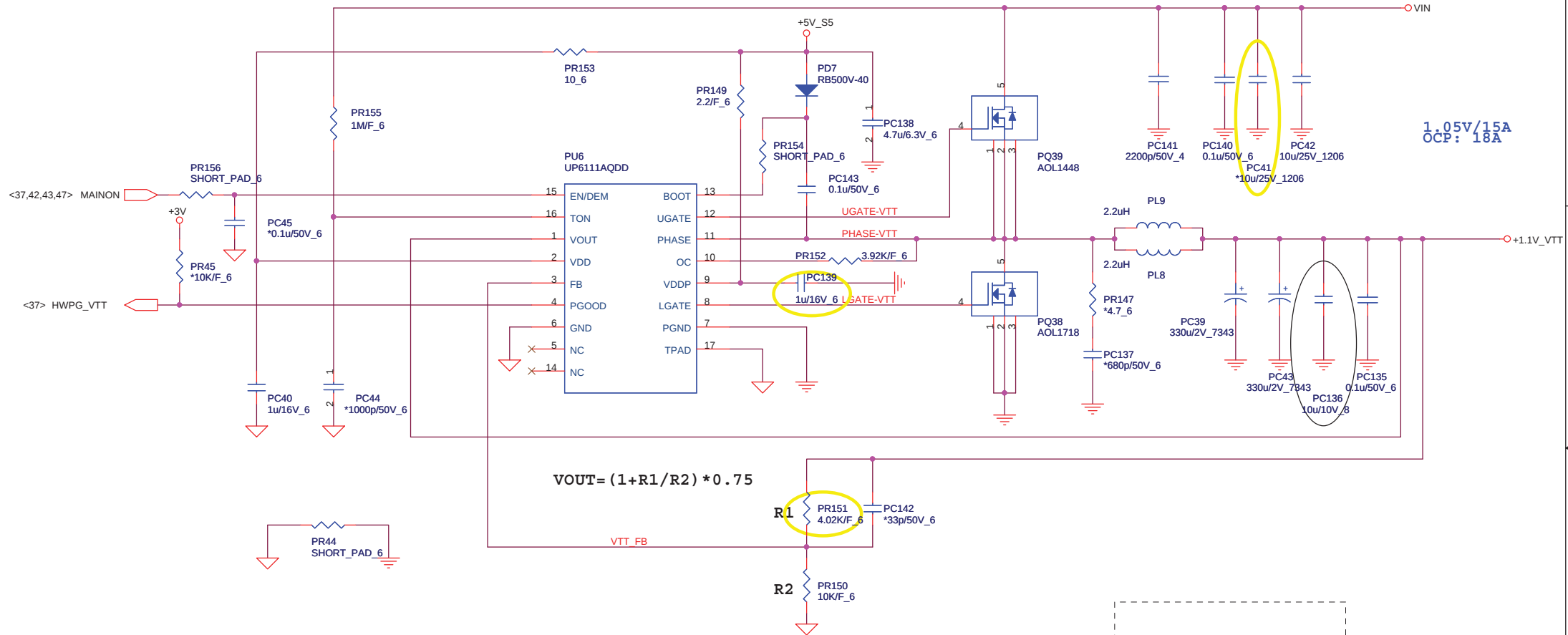


[PWM]

PR71, PR72, PR73, PR74, PR75, PR76, and PR77 deleted



[PWM]



$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

AO1718 Rdson = 3~4.3mOhm

$$L(ripple\ current) = (19 - 1.05) * 1.05 / (1u * 272k * 19) \sim 3.64A$$

$$4.3m * 18 = RILIM * 20uA$$

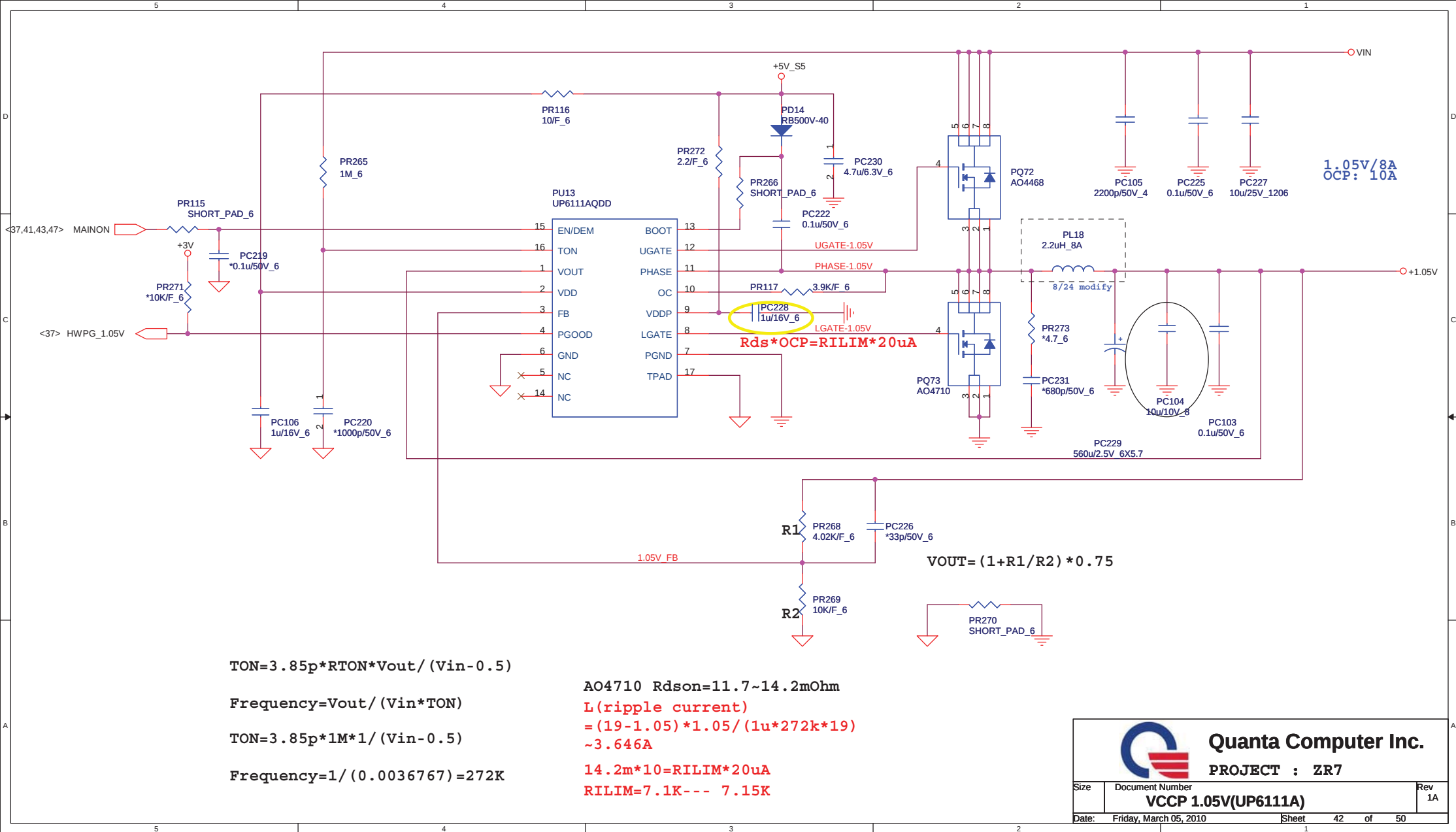
$$RILIM = 3.87K \text{ --- } 3.92K$$

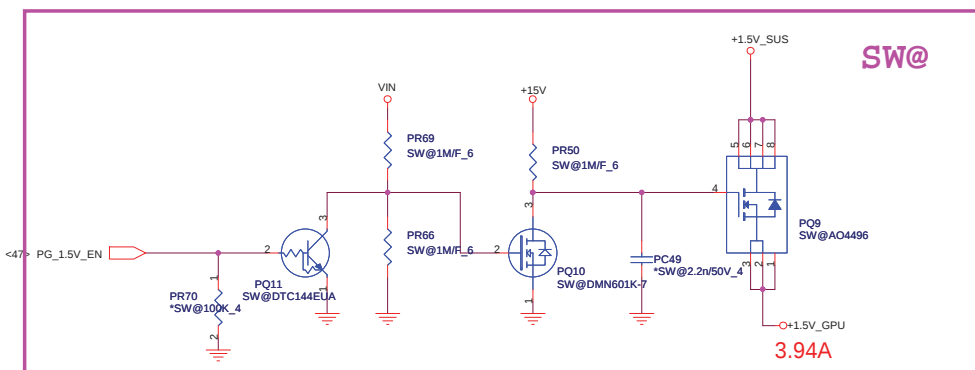
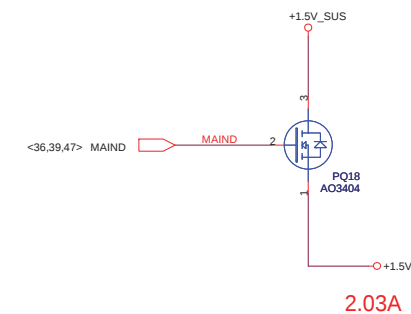
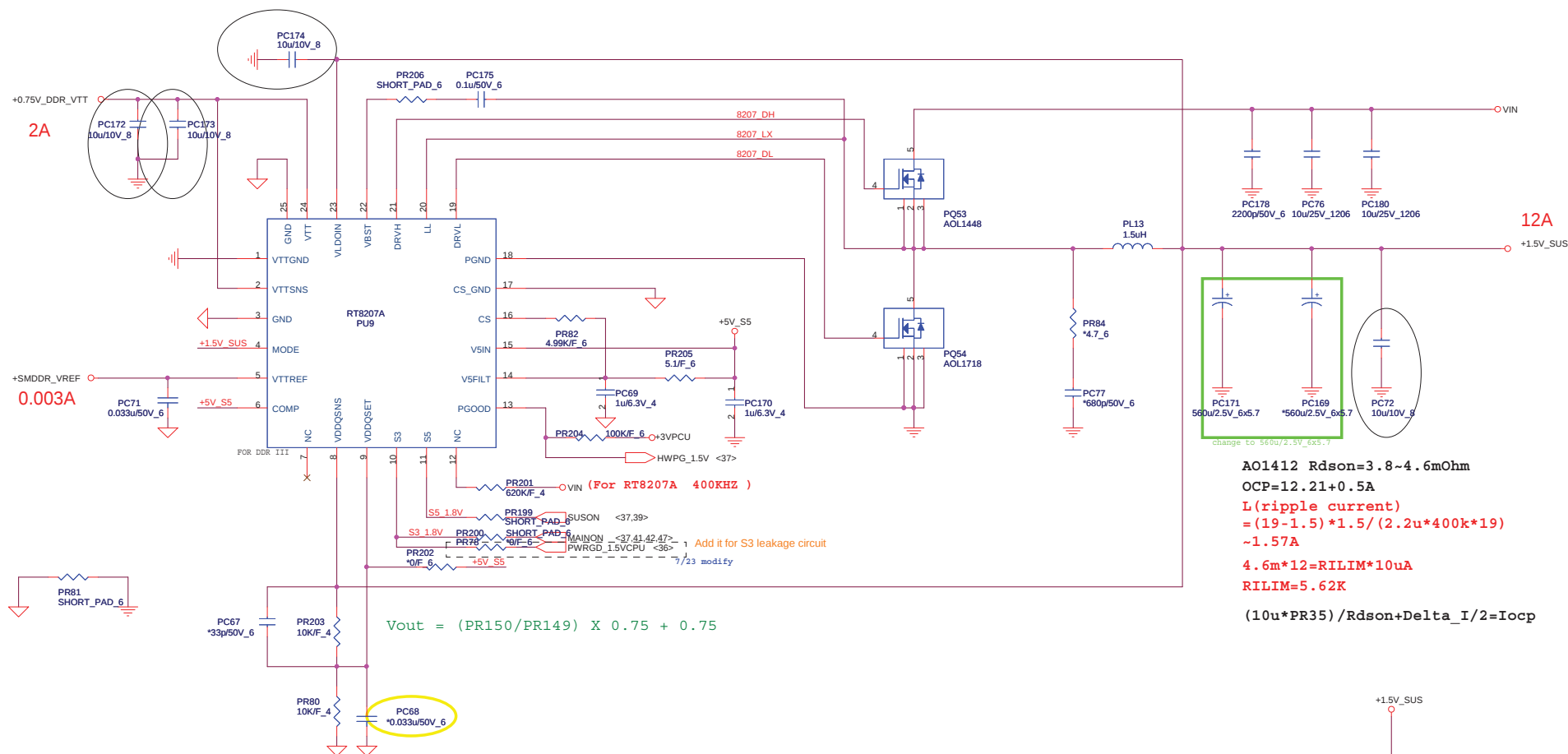


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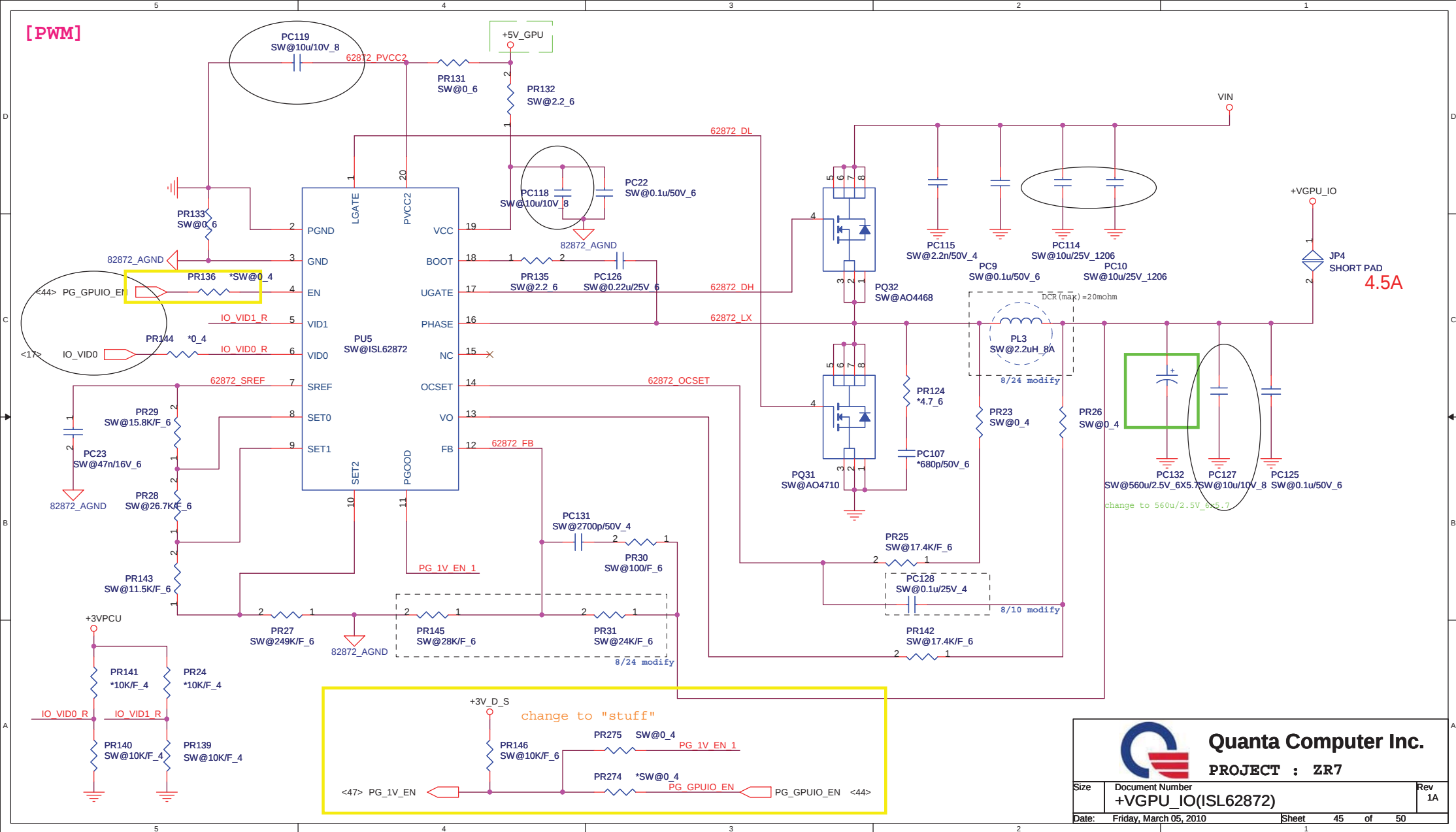
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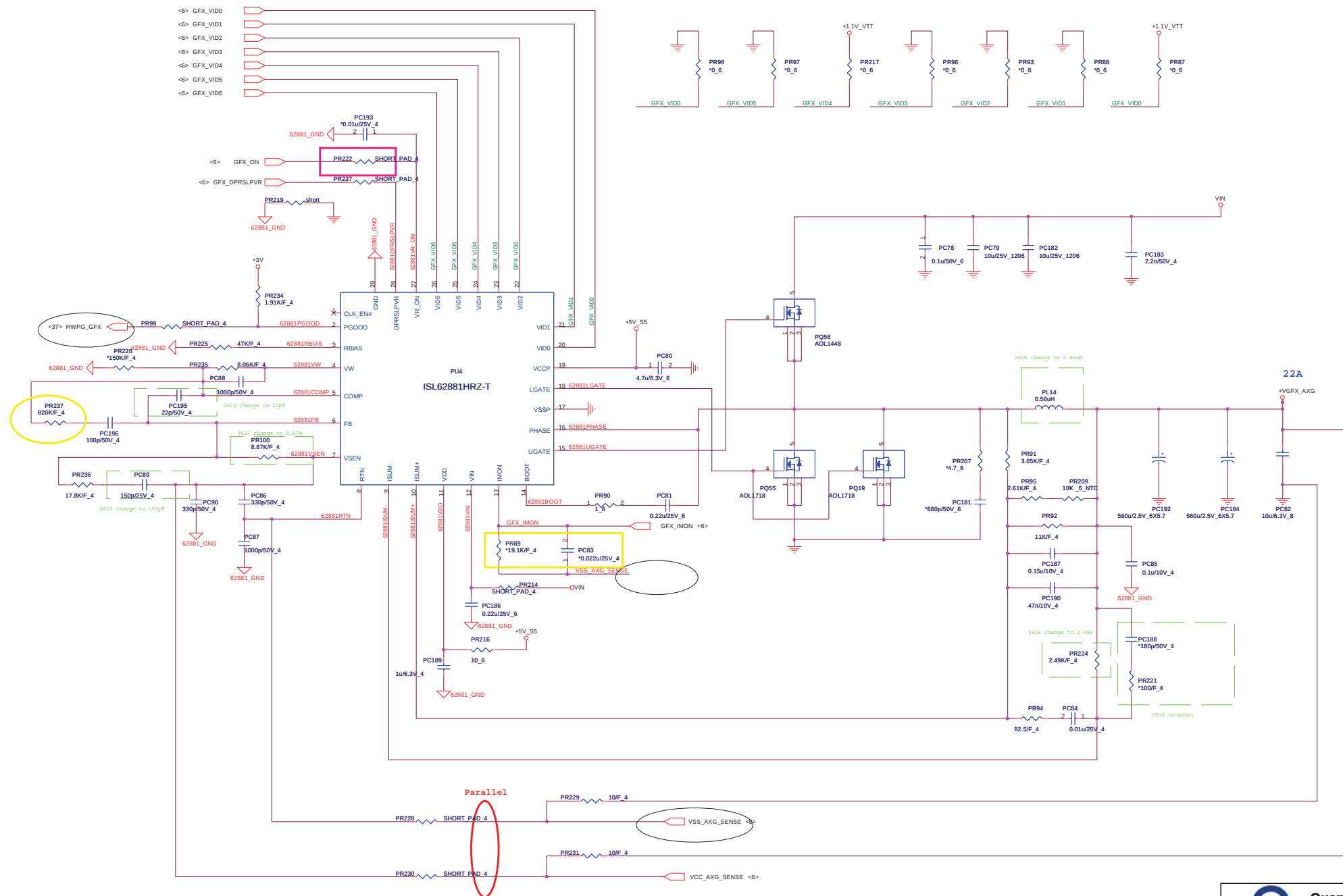
[PWM]



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DCR=1.6~1.8mOhm
Load Line=7mV/A
 $1.6\text{m} \times 0.6168 = 0.986\text{m}$
 $0.986\text{m} / .49\text{K} = 396\text{p}$
 $392\text{p} \times 2 \times 8.87\text{K} = 7.03\text{m}$
OCP
 $20\text{u} / 2 \times 2.49\text{K} = 24.9\text{m}$
 $24.9\text{m} / 0.6168 = 40.3\text{m}$
 $40.3\text{m} / 1.6\text{m} = 25.2\text{A}$

